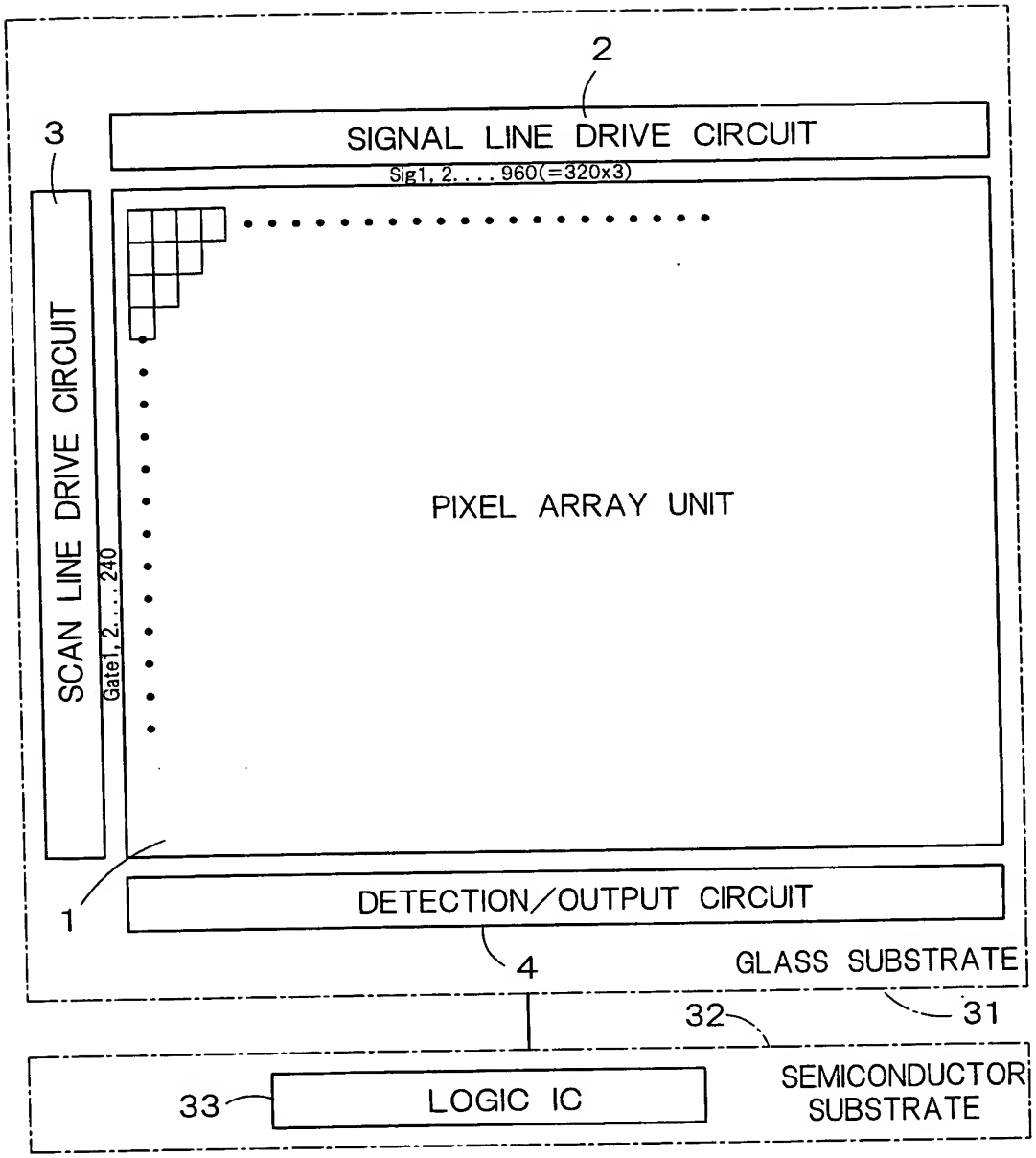

2
SIGNAL LINE DRIVE CIRCUIT
3
Sig1, 2. . . . 960(=320x3)
SCAN LINE DRIVE CIRCUIT
Gate1, 2. . . . 240
PIXEL ARRAY UNIT
1
DETECTION/OUTPUT CIRCUIT
4
GLASS SUBSTRATE
32
31
33
LOGIC IC
SEMICONDUCTOR SUBSTRATE

FIG. 1

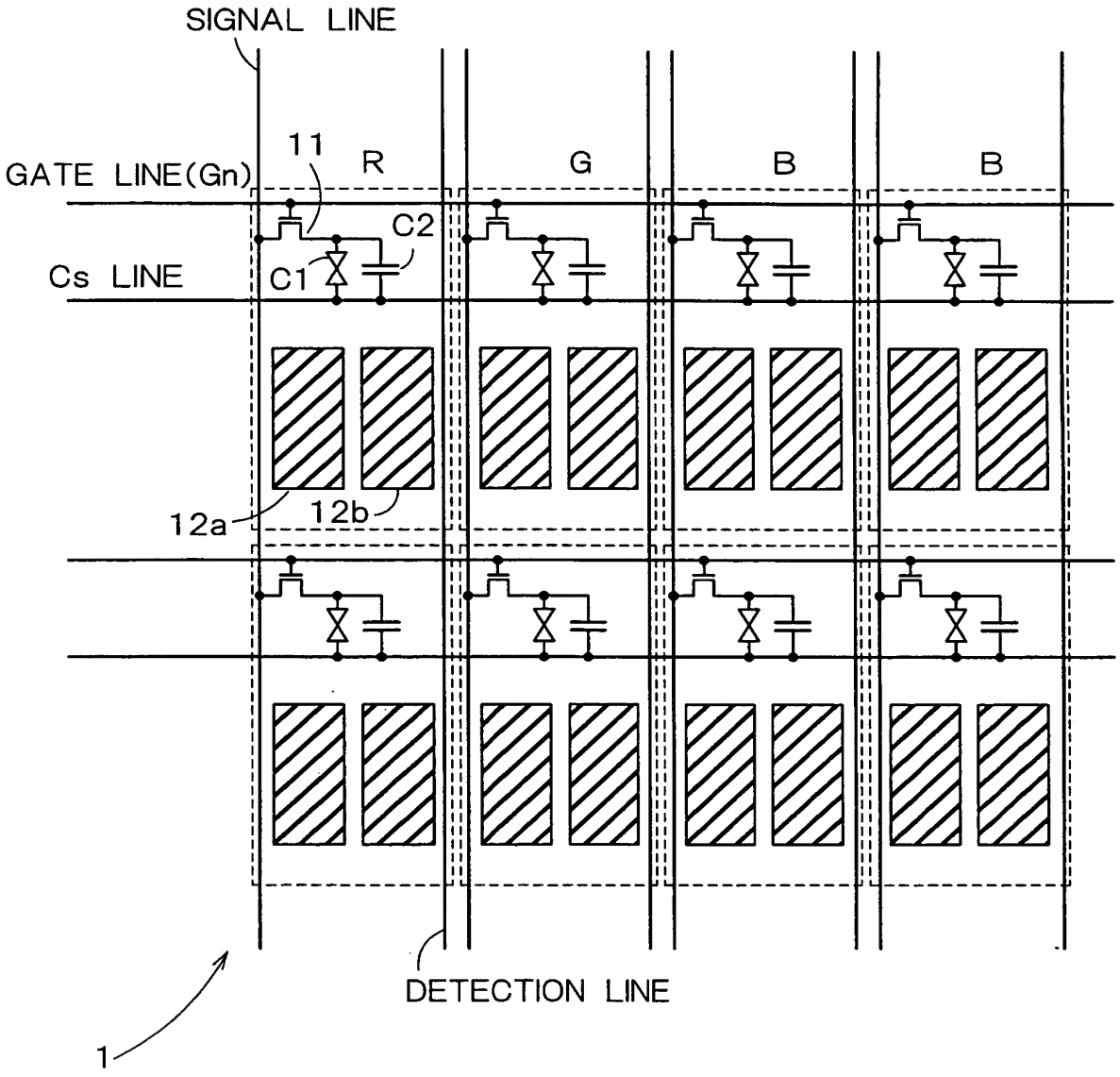

SIGNAL LINE
GATE LINE(Gn)
11
R
G
B
B
C2
C1
Cs LINE
12a
12b
DETECTION LINE
1

FIG. 2

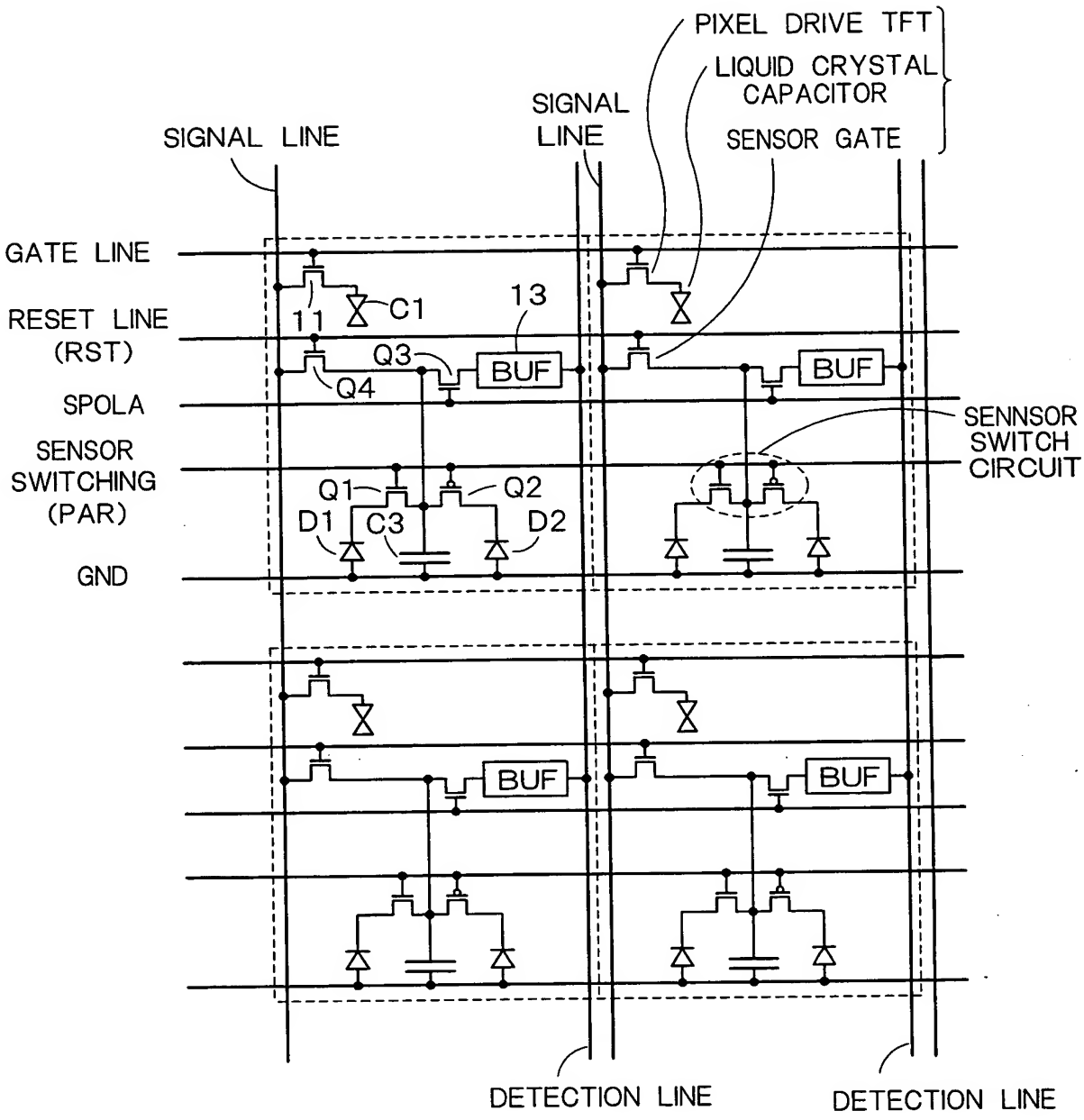

PIXEL DRIVE TFT
LIQUID CRYSTAL CAPACITOR
SENSOR GATE
SIGNAL LINE
SIGNAL LINE
GATE LINE
RESET LINE (RST)
SPOLA
SENSOR SWITCHING (PAR)
GND
11
C1
13
Q3
Q4
BUF
BUF
SENNSOR SWITCH CIRCUIT
Q1
Q2
D1
C3
D2
BUF
BUF
DETECTION LINE
DETECTION LINE

FIG. 3

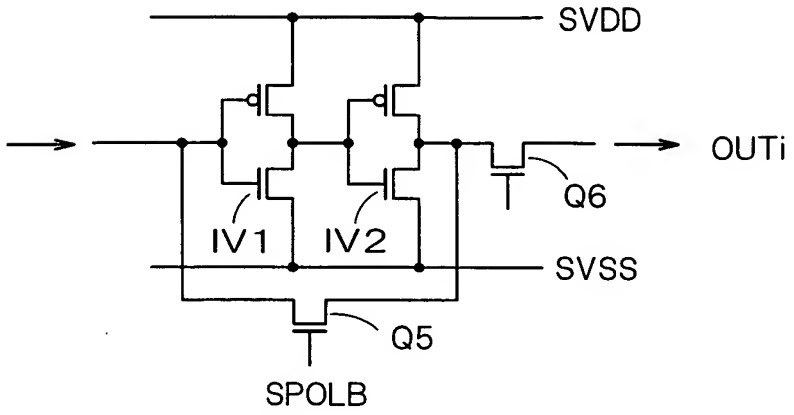

SVDD
OUTi
Q6
IV1
IV2
SVSS
Q5
SPOLB

FIG. 4

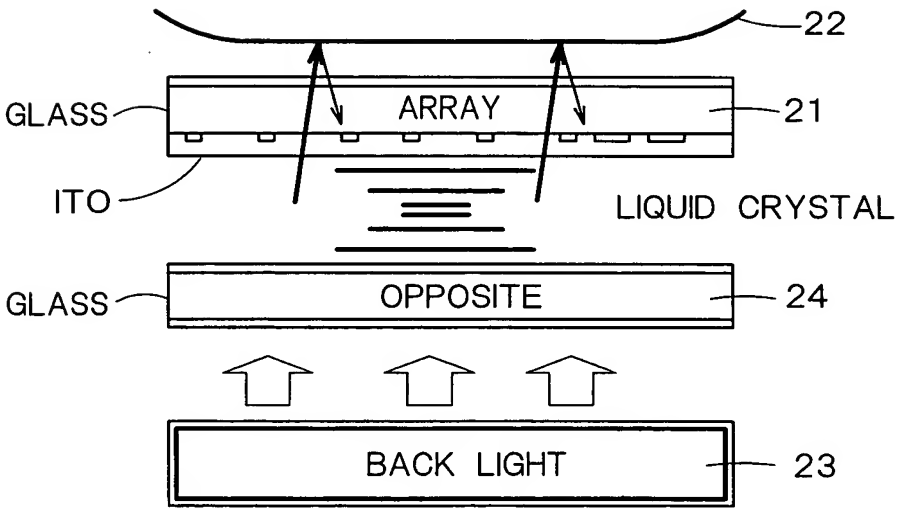

22
GLASS
ARRAY
21
ITO
LIQUID CRYSTAL
GLASS
OPPOSITE
24
BACK LIGHT
23

FIG. 5

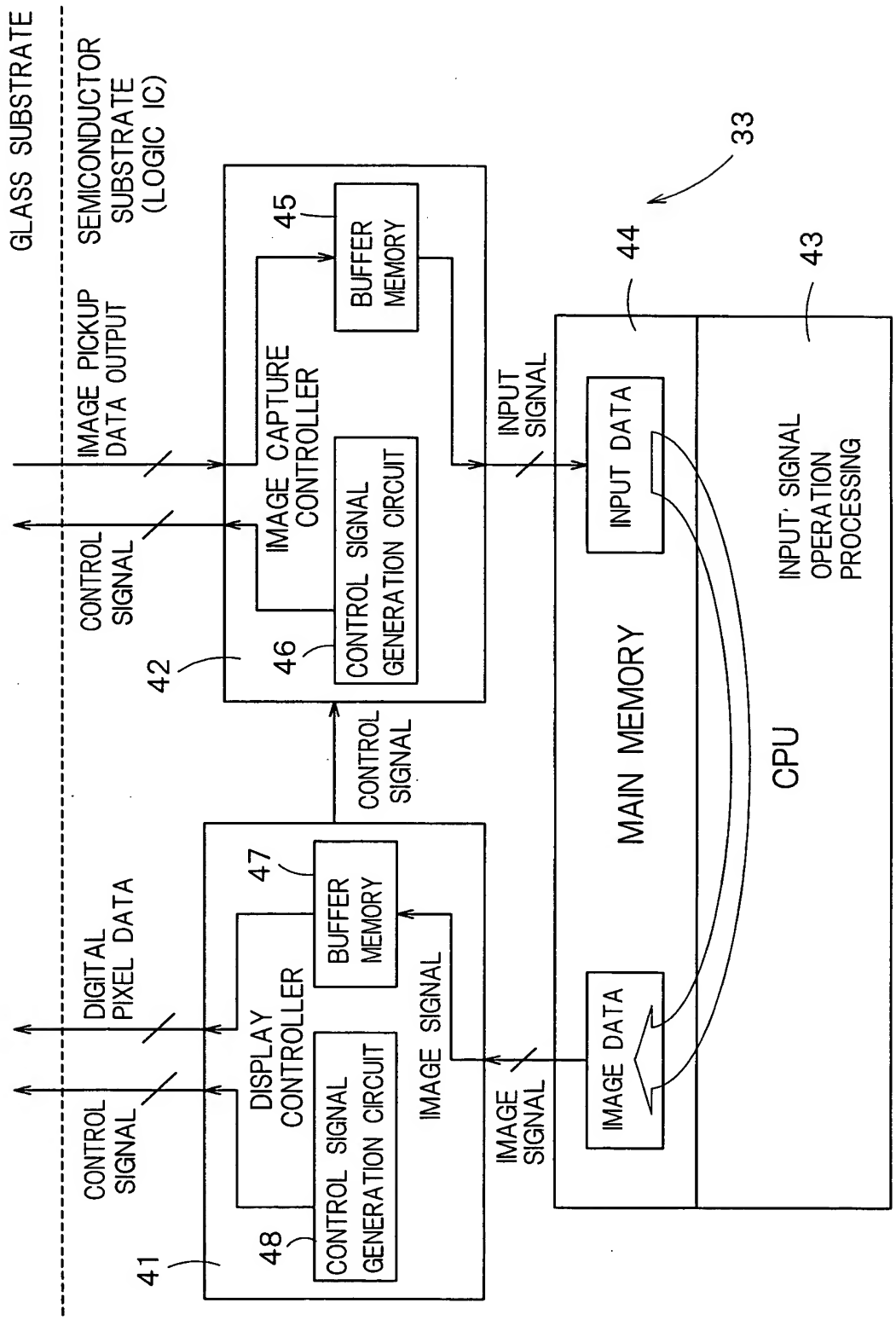

GLASS SUBSTRATE
SEMICONDUCTOR SUBSTRATE (LOGIC IC)
IMAGE PICKUP DATA OUTPUT
CONTROL SIGNAL
IMAGE CAPTURE CONTROLLER
BUFFER MEMORY
CONTROL SIGNAL GENERATION CIRCUIT
42
45
46
CONTROL SIGNAL
INPUT SIGNAL
33
44
43
INPUT DATA
MAIN MEMORY
CPU
INPUT' SIGNAL OPERATION PROCESSING
DIGITAL PIXEL DATA
DISPLAY CONTROLLER
BUFFER MEMORY
CONTROL SIGNAL GENERATION CIRCUIT
IMAGE SIGNAL
IMAGE DATA
41
47
48

FIG. 6

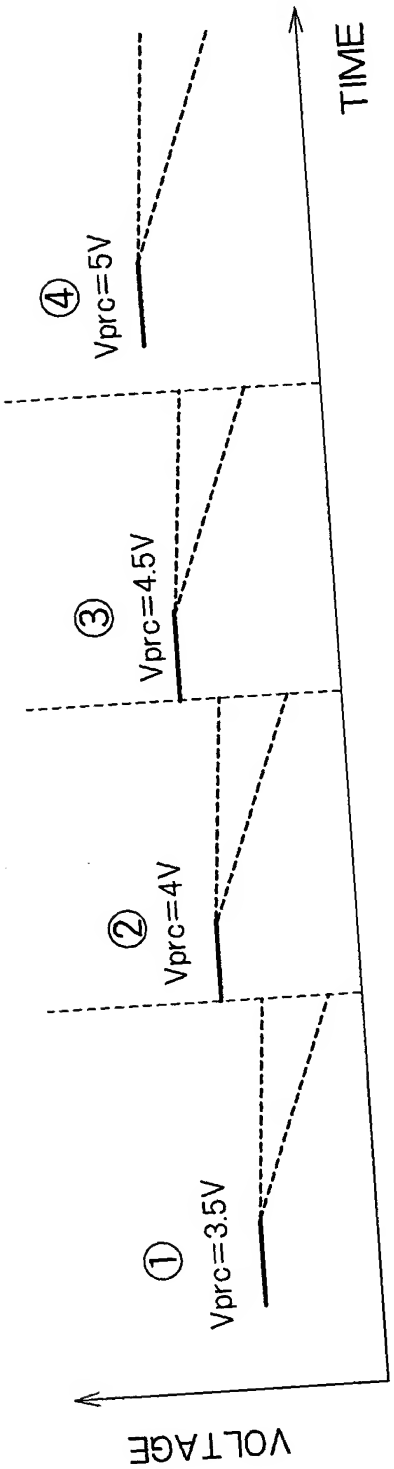


FIG. 7

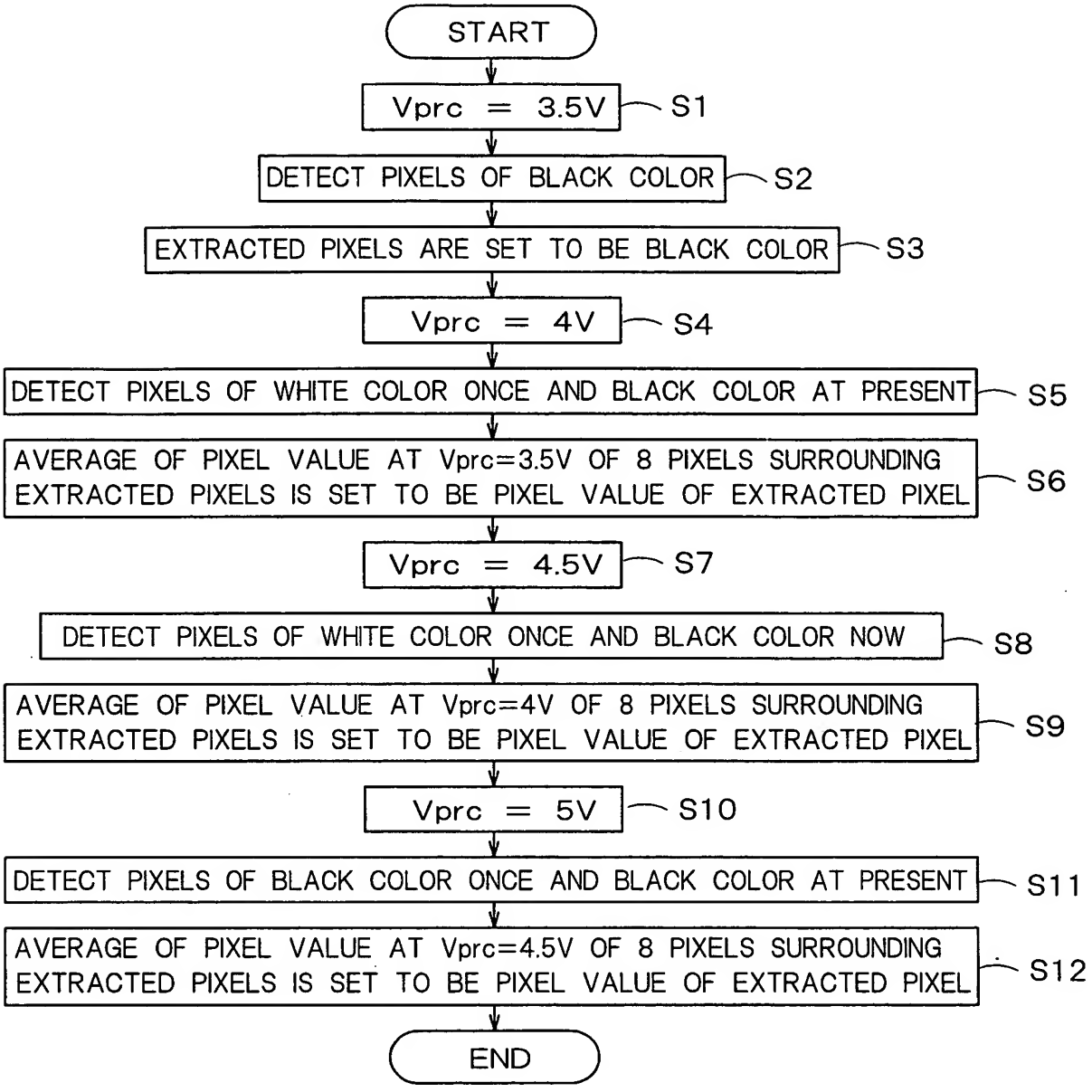
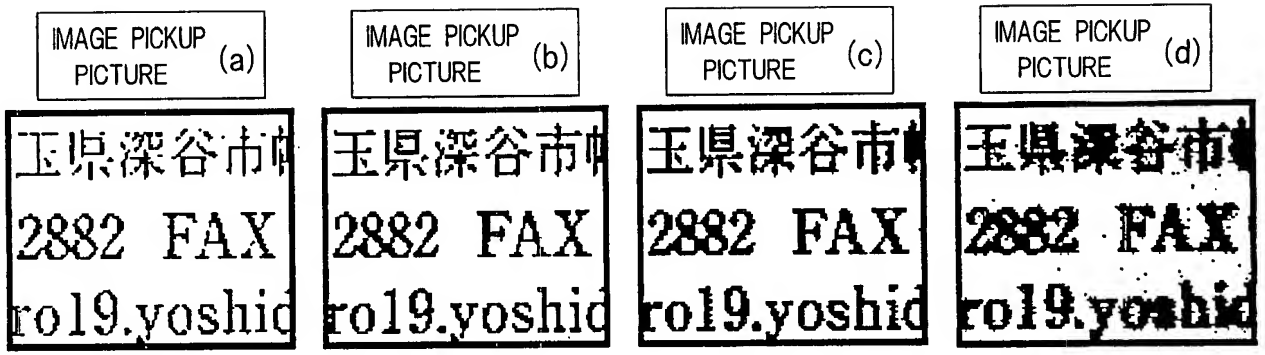

START
Vprc = 3.5V
S1
DETECT PIXELS OF BLACK COLOR
S2
EXTRACTED PIXELS ARE SET TO BE BLACK COLOR
S3
Vprc = 4V
S4
DETECT PIXELS OF WHITE COLOR ONCE AND BLACK COLOR AT PRESENT
S5
AVERAGE OF PIXEL VALUE AT Vprc=3.5V OF 8 PIXELS SURROUNDING EXTRACTED PIXELS IS SET TO BE PIXEL VALUE OF EXTRACTED PIXEL
S6
Vprc = 4.5V
S7
DETECT PIXELS OF WHITE COLOR ONCE AND BLACK COLOR NOW
S8
AVERAGE OF PIXEL VALUE AT Vprc=4V OF 8 PIXELS SURROUNDING EXTRACTED PIXELS IS SET TO BE PIXEL VALUE OF EXTRACTED PIXEL
S9
Vprc = 5V
S10
DETECT PIXELS OF BLACK COLOR ONCE AND BLACK COLOR AT PRESENT
S11
AVERAGE OF PIXEL VALUE AT Vprc=4.5V OF 8 PIXELS SURROUNDING EXTRACTED PIXELS IS SET TO BE PIXEL VALUE OF EXTRACTED PIXEL
S12
END

FIG. 8



CHANGING PARAMETER	CONDITION (a)	CONDITION (b)	CONDITION (c)	CONDITION (d)
PRECHARGE VOLTAGE(V) OF CAPACITOR	3.5	4.0	4.5	5.0
IMAGE PICKUP TIME (ms)	100	75	50	25
TRANSMITTANCE (%) OF LIQUID CRYSTAL	100	75	50	25
SUMMARY	CONDITION THAT ONLY PORTIONS NEAR TO CONSIDERABLY BLACK ARE DITERMINED AS BLACK	⟷		CONDITION THAT ONLY PORTIONS NEAR TO CONSIDERABLY WHITE ARE DITERMINED AS WHITE

FIG. 9

OBLON, SPIVAK, ET AL
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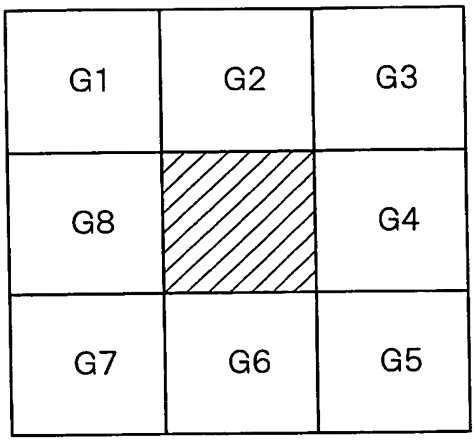


FIG. 10

県深谷市
2882 FAX
ro19.yoshid

FIG. 11

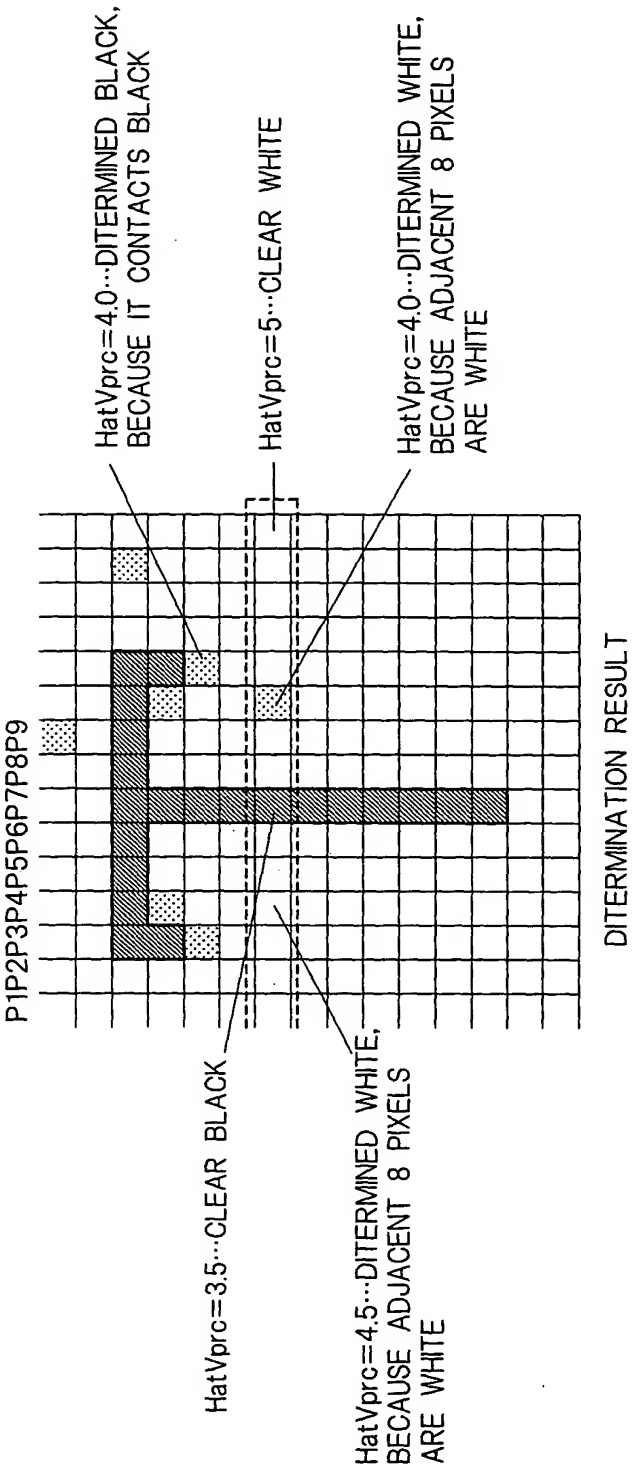
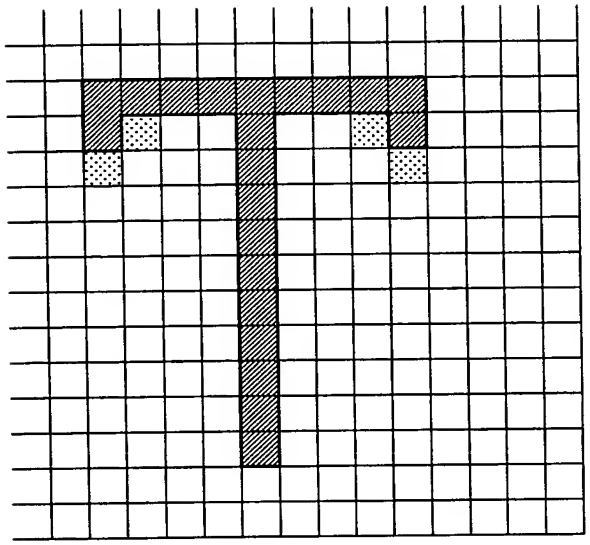

HatVprc=4.0···DITERMINED BLACK, BECAUSE IT CONTACTS BLACK
HatVprc=5···CLEAR WHITE
HatVprc=4.0···DITERMINED WHITE, BECAUSE ADJACENT 8 PIXELS ARE WHITE
P1P2P3P4P5P6P7P8P9
DITERMINATION RESULT
HatVprc=3.5···CLEAR BLACK
HatVprc=4.5···DITERMINED WHITE, BECAUSE ADJACENT 8 PIXELS ARE WHITE

FIG. 12

Vprc(V)	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15
(a) 3.5	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
(b) 4.0	L	L	L	L	L	L	H	L	L	H	L	L	L	L	L
(c) 4.5	L	L	L	H	L	L	H	L	L	H	L	L	L	L	L
(d) 5.0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

FIG. 13



REPRODUCED IMAGE ON DISPLAY DEVICE

FIG. 14

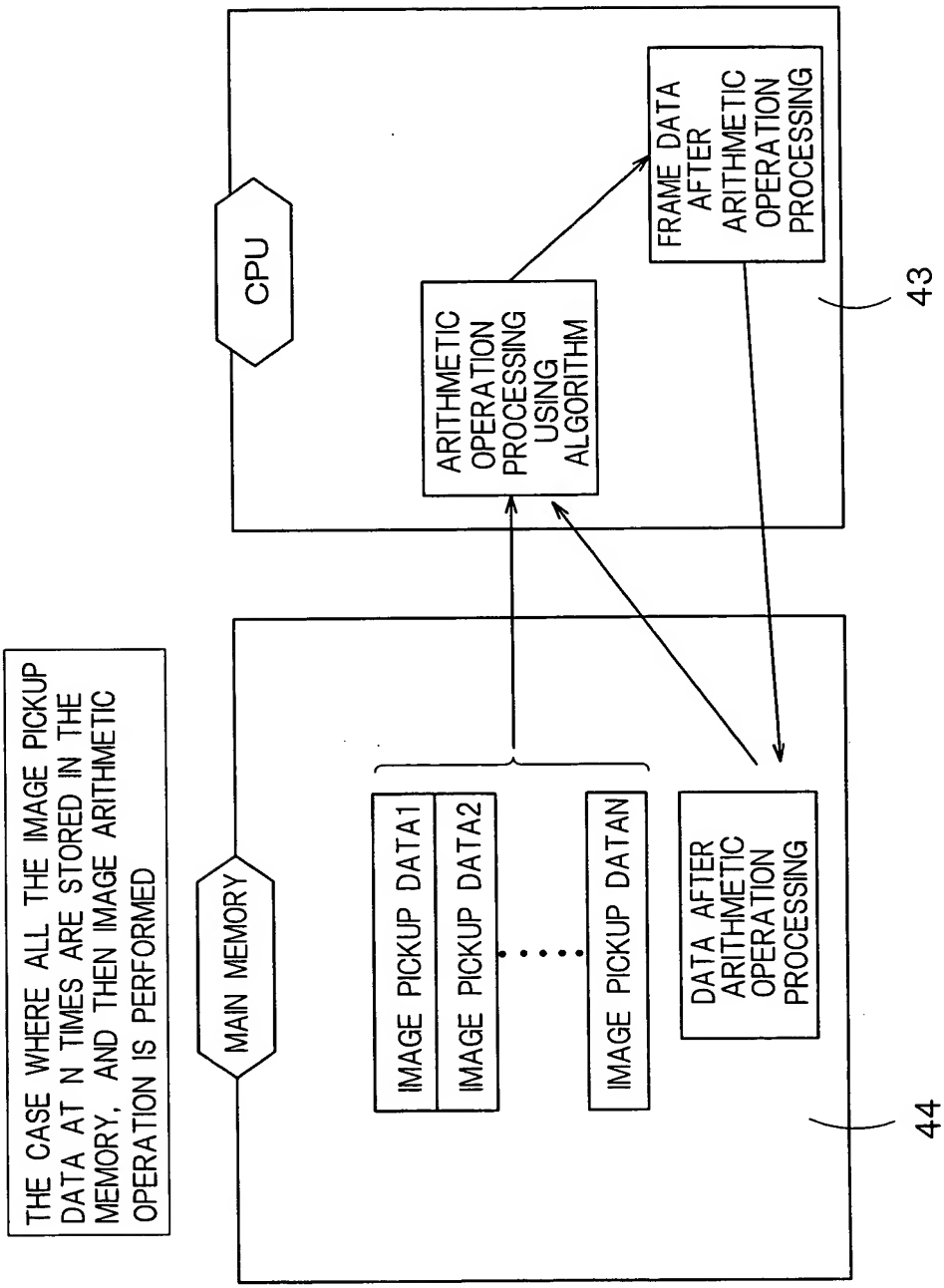

CPU
ARITHMETIC OPERATION PROCESSING USING ALGORITHM
FRAME DATA AFTER ARITHMETIC OPERATION PROCESSING
43
MAIN MEMORY
IMAGE PICKUP DATA1
IMAGE PICKUP DATA2
IMAGE PICKUP DATAN
DATA AFTER ARITHMETIC OPERATION PROCESSING
44
THE CASE WHERE ALL THE IMAGE PICKUP DATA AT N TIMES ARE STORED IN THE MEMORY, AND THEN IMAGE ARITHMETIC OPERATION IS PERFORMED

FIG. 15

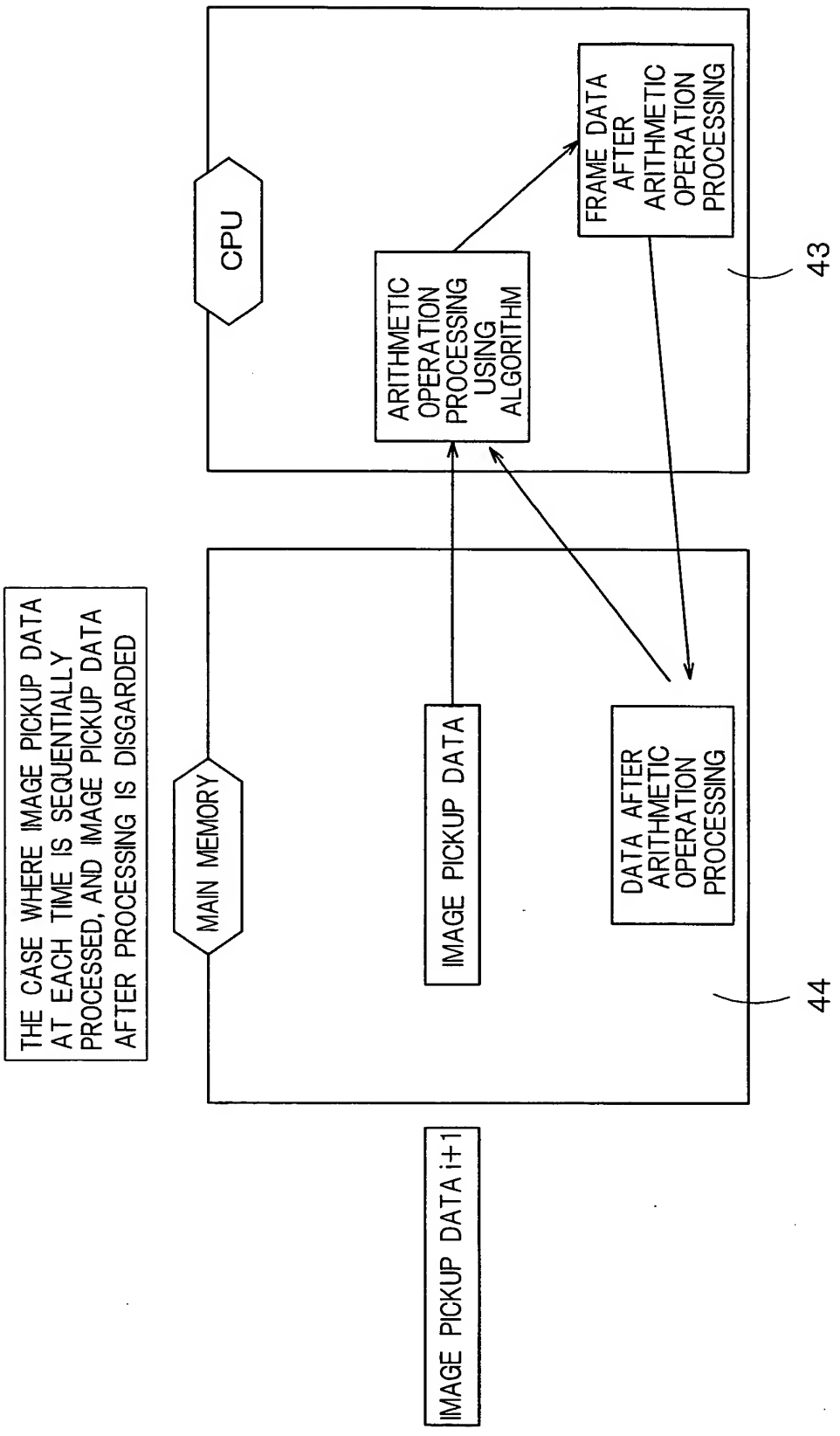

CPU
ARITHMETIC OPERATION PROCESSING USING ALGORITHM
FRAME DATA AFTER ARITHMETIC OPERATION PROCESSING
43
MAIN MEMORY
IMAGE PICKUP DATA
DATA AFTER ARITHMETIC OPERATION PROCESSING
44
IMAGE PICKUP DATA i+1
THE CASE WHERE IMAGE PICKUP DATA AT EACH TIME IS SEQUENTIALLY PROCESSED, AND IMAGE PICKUP DATA AFTER PROCESSING IS DISGARDED

FIG. 16

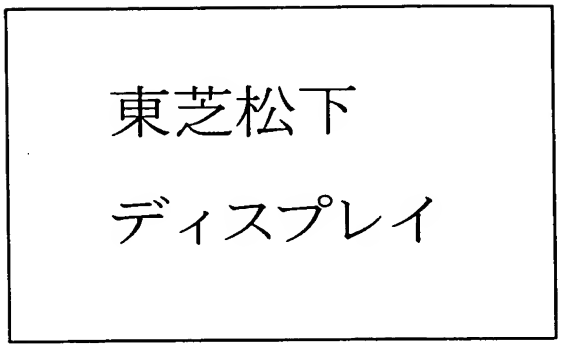


FIG. 17A

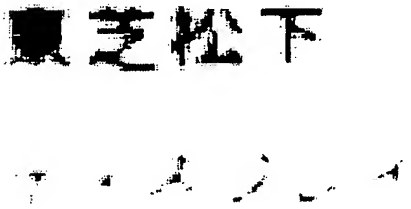


FIG. 17B

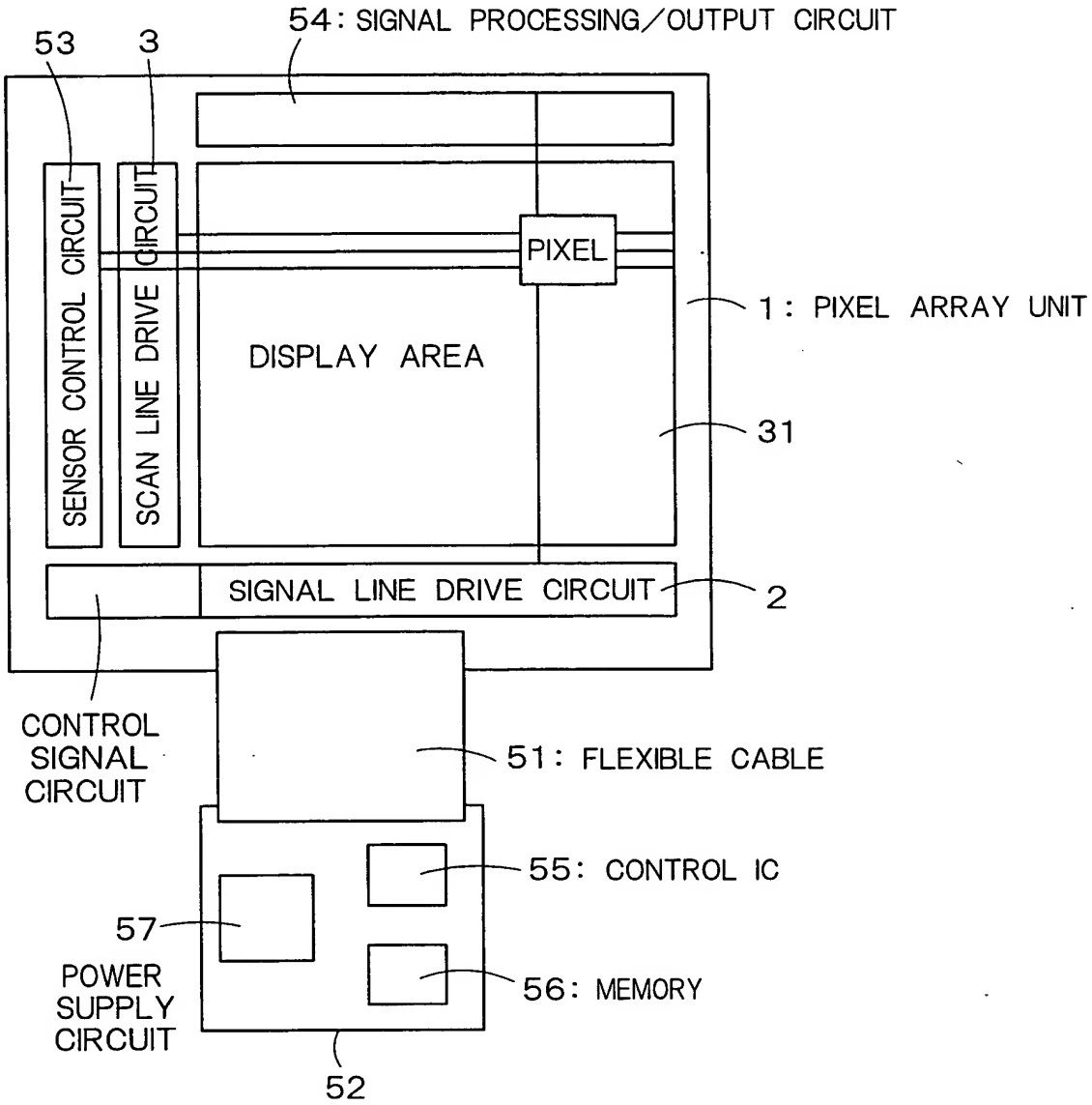

54: SIGNAL PROCESSING/OUTPUT CIRCUIT
53
3
SENSOR CONTROL CIRCUIT
SCAN LINE DRIVE CIRCUIT
PIXEL
1: PIXEL ARRAY UNIT
DISPLAY AREA
31
SIGNAL LINE DRIVE CIRCUIT
2
CONTROL SIGNAL CIRCUIT
51: FLEXIBLE CABLE
55: CONTROL IC
57
POWER SUPPLY CIRCUIT
56: MEMORY
52

FIG. 18

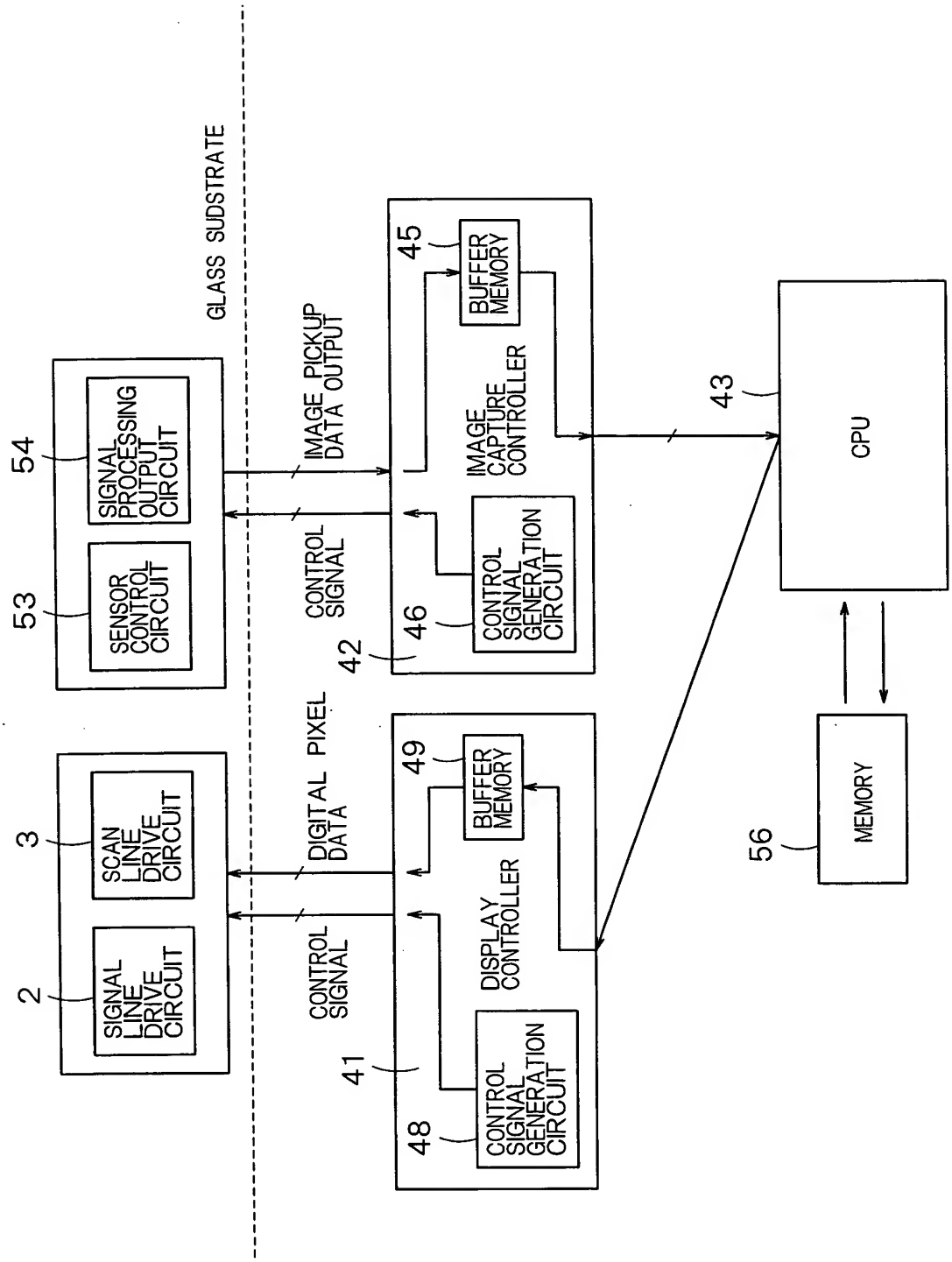

GLASS SUBSTRATE
SIGNAL LINE DRIVE CIRCUIT
SCAN LINE DRIVE CIRCUIT
SENSOR CONTROL CIRCUIT
SIGNAL PROCESSING OUTPUT CIRCUIT
DIGITAL PIXEL DATA
CONTROL SIGNAL
IMAGE PICKUP DATA OUTPUT
CONTROL SIGNAL
DISPLAY CONTROLLER
CONTROL SIGNAL GENERATION CIRCUIT
BUFFER MEMORY
IMAGE CAPTURE CONTROLLER
CONTROL SIGNAL GENERATION CIRCUIT
BUFFER MEMORY
CPU
MEMORY
2
3
53
54
41
48
49
42
46
45
43
56

FIG. 19

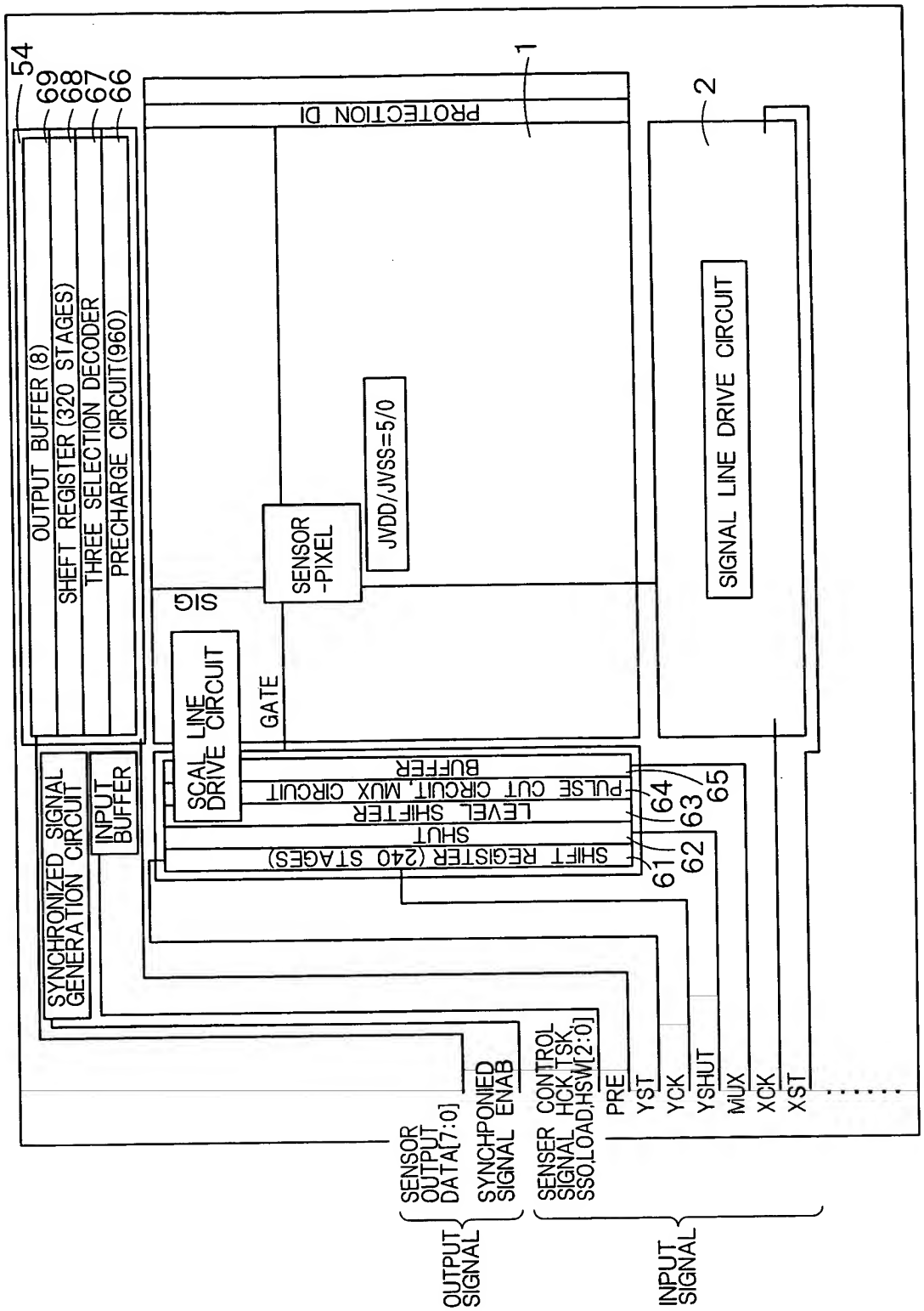

54
69
68
67
66
OUTPUT BUFFER (8)
SHEFT REGISTER (320 STAGES)
THREE SELECTION DECODER
PRECHARGE CIRCUIT(960)
1
PROTECTION DI
2
SIGNAL LINE DRIVE CIRCUIT
SENSOR -PIXEL
JVDD/JVSS=5/0
SIG
SCAL LINE DRIVE CIRCUIT
GATE
SYNCHRONIZED SIGNAL GENERATION CIRCUIT
INPUT BUFFER
BUFFER
PULSE CUT CIRCUIT, MUX CIRCUIT
LEVEL SHIFTER
SHUT
SHIFT REGISTER (240 STAGES)
61
62
63
64
65
SENSOR OUTPUT DATA[7:0]
SYNCHRONIED SIGNAL ENAB
SENSER CONTROL SIGNAL HCK,TSK, SSO,LOAD,HSW[2:0]
PRE
YST
YCK
YSHUT
MUX
XCK
XST
OUTPUT SIGNAL
INPUT SIGNAL

FIG. 20

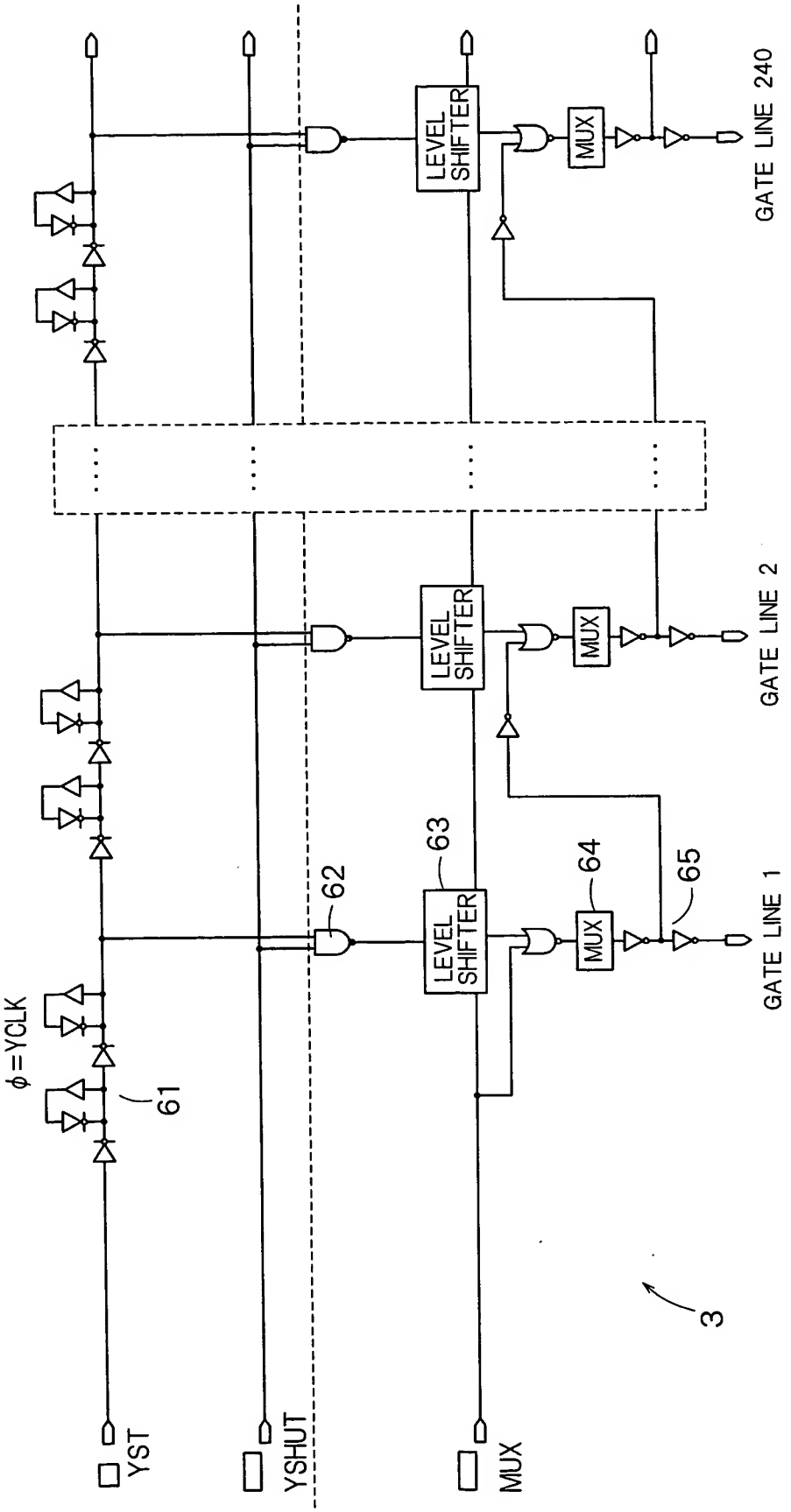

LEVEL SHIFTER
MUX
GATE LINE 240
GATE LINE 2
GATE LINE 1
63
64
65
62
61
φ=YCLK
YST
YSHUT
MUX
3

FIG. 21

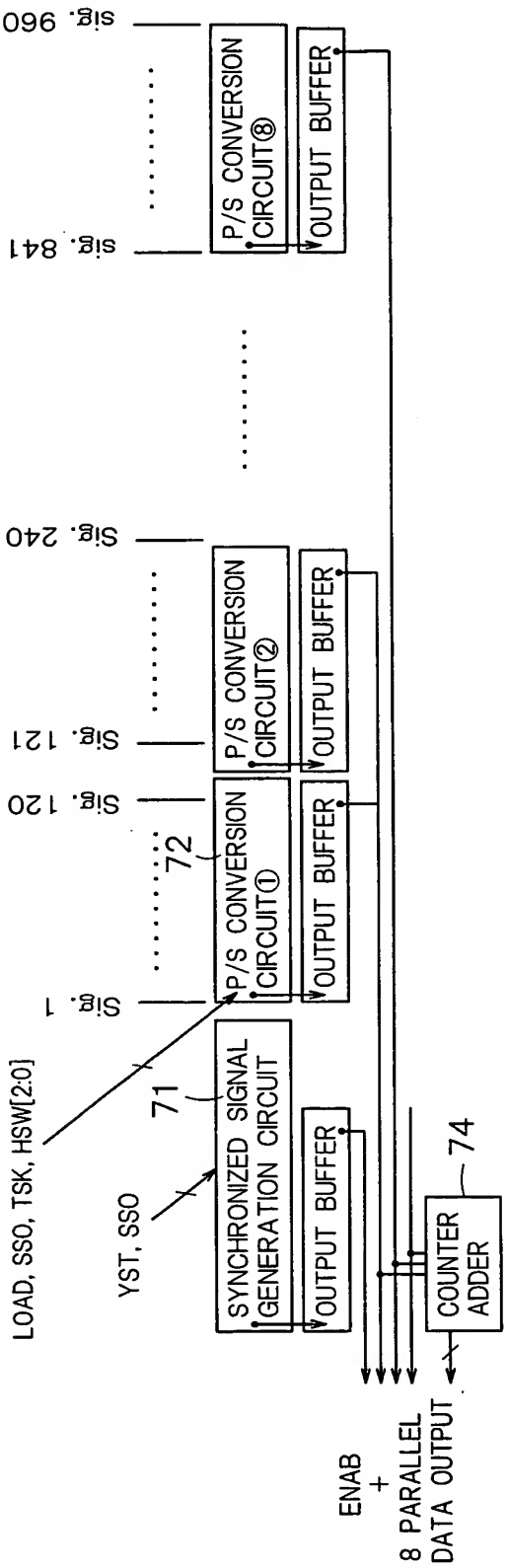

Sig. 960
Sig. 841
Sig. 240
Sig. 121
Sig. 120
Sig. 1
P/S CONVERSION CIRCUIT⑧
P/S CONVERSION CIRCUIT②
P/S CONVERSION CIRCUIT①
OUTPUT BUFFER
OUTPUT BUFFER
OUTPUT BUFFER
OUTPUT BUFFER
72
71
74
SYNCHRONIZED SIGNAL GENERATION CIRCUIT
COUNTER ADDER
LOAD, SSO, TSK, HSW[2:0]
YST, SSO
ENAB
+
8 PARALLEL DATA OUTPUT
54

FIG. 22

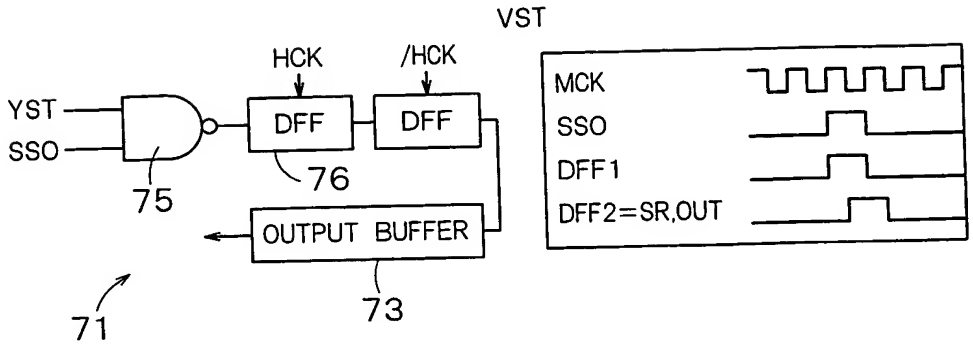
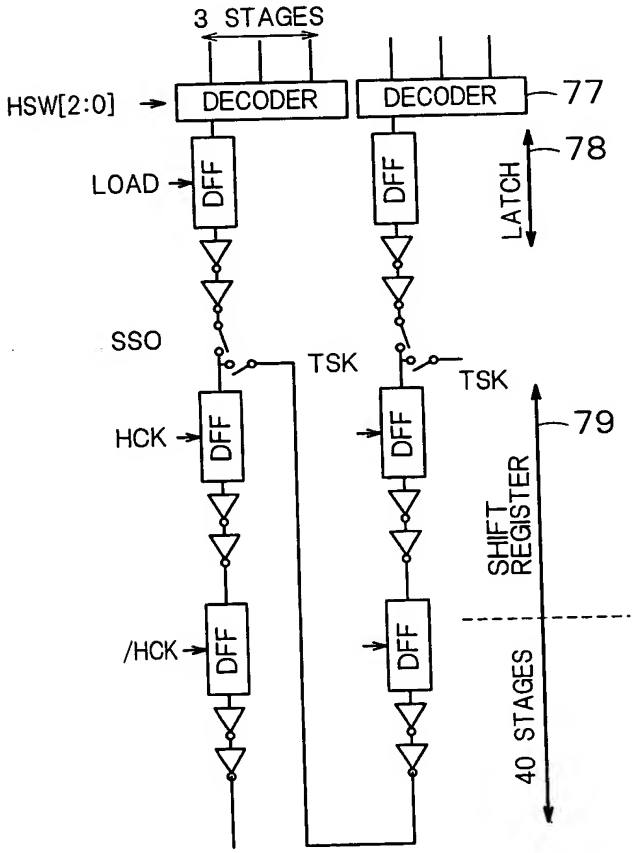


FIG. 23



72

FIG. 24

22 / 57

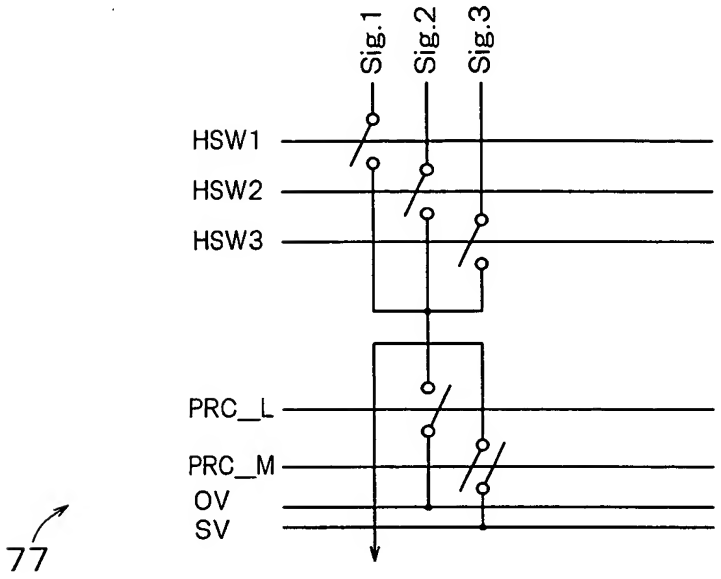


FIG. 25

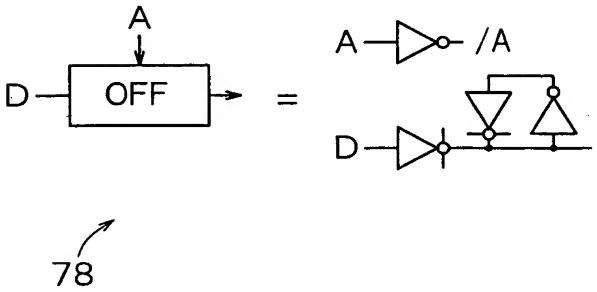


FIG. 26

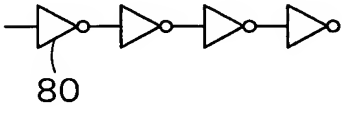
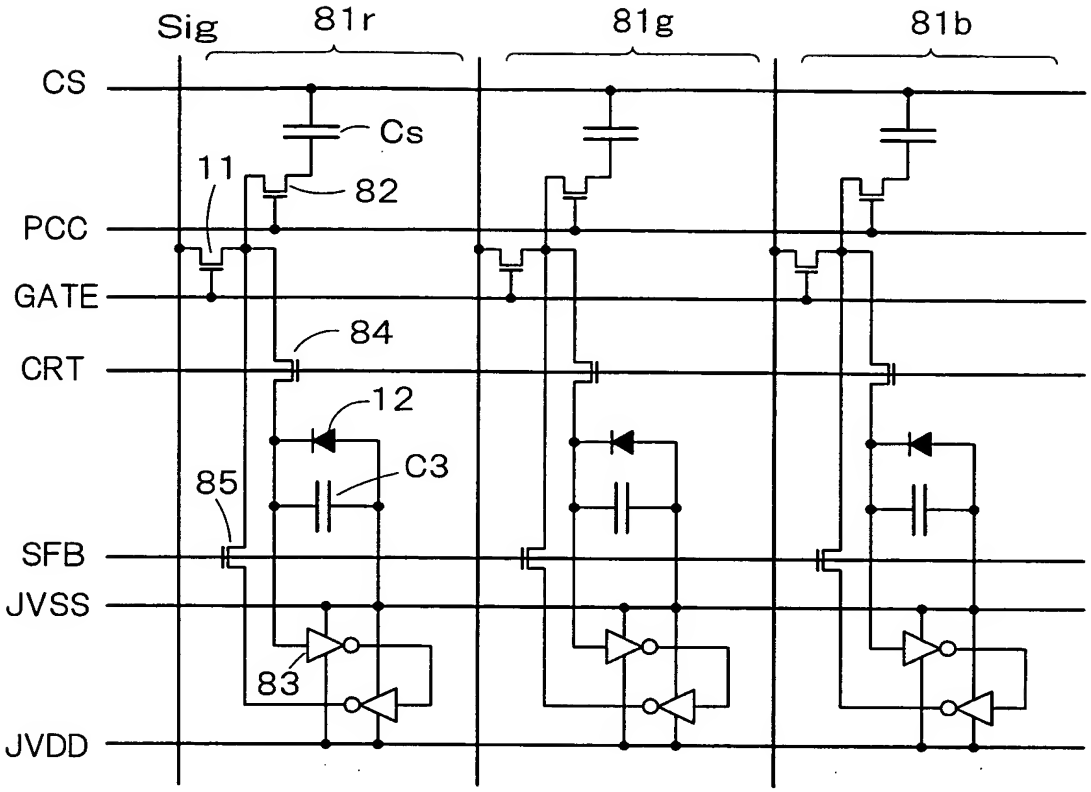


FIG. 27



PCC···PIXEL Cs CONNECTION

SFB···SRAM FEED BACK

CRT···CAPACITOR RESET TRANSISTOR

FIG. 28

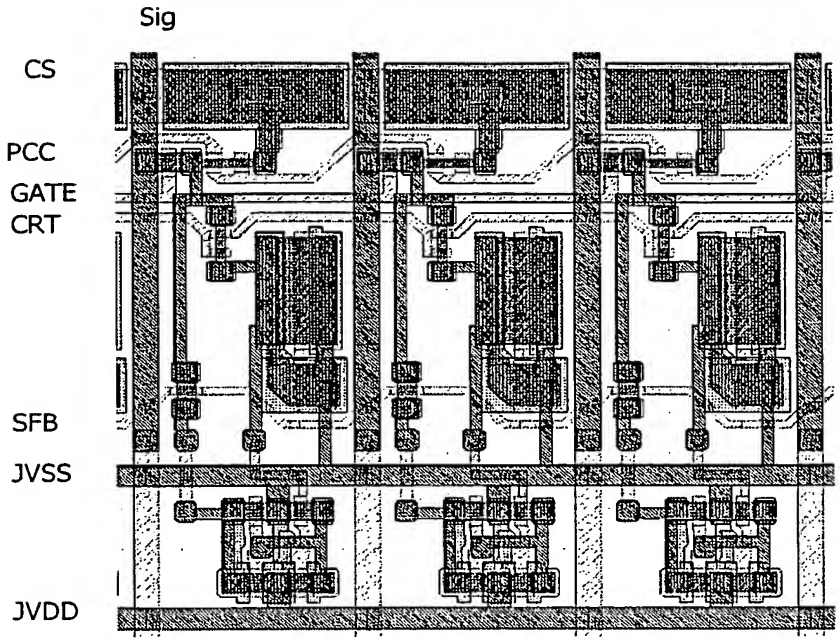


FIG. 29

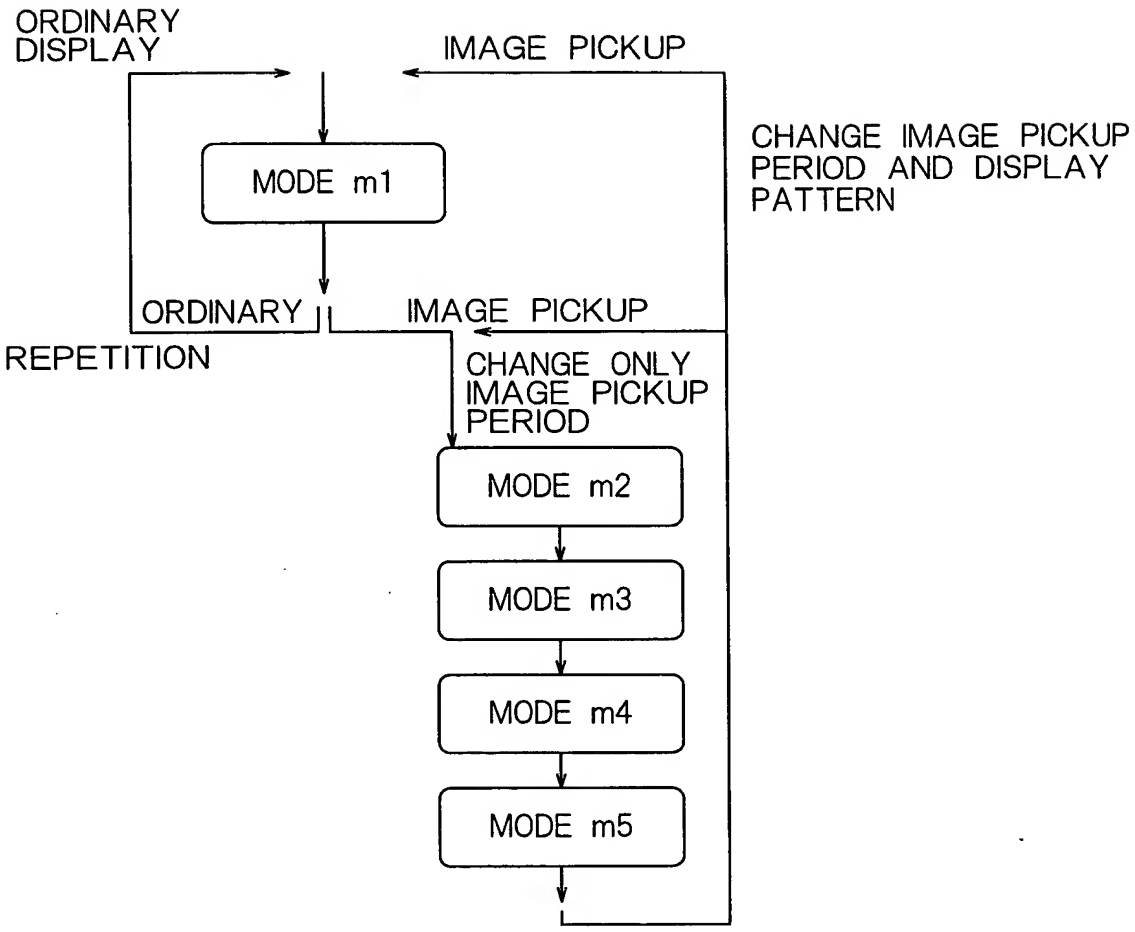

ORDINARY DISPLAY
IMAGE PICKUP
CHANGE IMAGE PICKUP PERIOD AND DISPLAY PATTERN
MODE m1
ORDINARY
IMAGE PICKUP
REPETITION
CHANGE ONLY IMAGE PICKUP PERIOD
MODE m2
MODE m3
MODE m4
MODE m5

FIG. 30

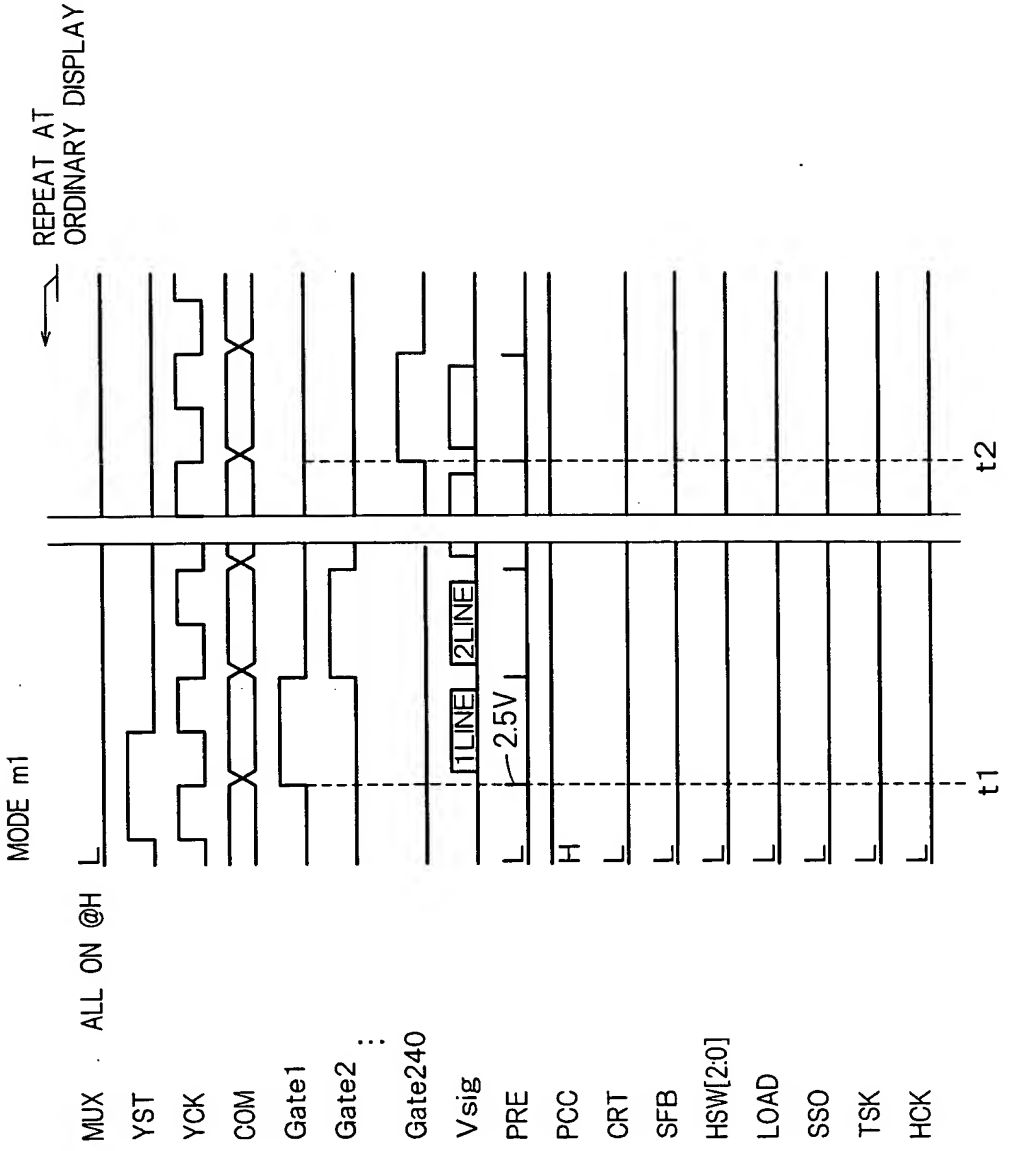

REPEAT AT
ORDINARY DISPLAY
MODE m1
MUX
ALL ON @H
YST
YCK
COM
Gate1
Gate2
Gate240
Vsig
PRE
PCC
CRT
SFB
HSW[2:0]
LOAD
SSO
TSK
HCK
1LINE
2LINE
2.5V
t1
t2
L
H

FIG. 31

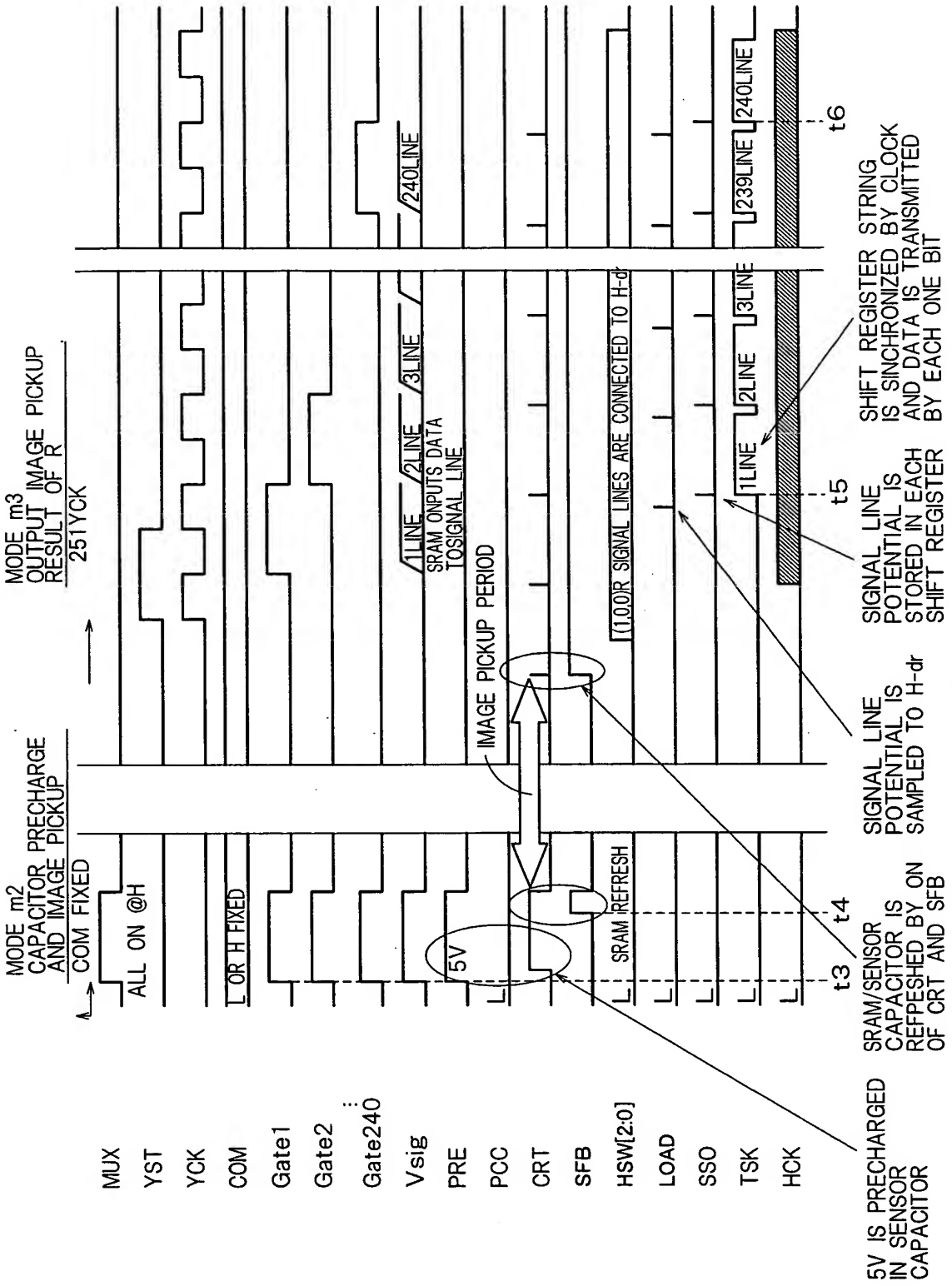

MODE m3
OUTPUT IMAGE PICKUP RESULT OF R
251YCK
MODE m2
CAPACITOR PRECHARGE AND IMAGE PICKUP
COM FIXED
ALL ON @H
L OR H FIXED
5V
IMAGE PICKUP PERIOD
SRAM REFRESH
1LINE
2LINE
3LINE
240LINE
SRAM ONPUTS DATA TOSIGNAL LINE
(1,0,0)R SIGNAL LINES ARE CONNECTED TO H-dr
239LINE
240LINE
1LINE
2LINE
3LINE
t3
t4
t5
t6
MUX
YST
YCK
COM
Gate1
Gate2
Gate240
Vsig
PRE
PCC
CRT
SFB
HSW[2:0]
LOAD
SSO
TSK
HCK
5V IS PRECHARGED IN SENSOR CAPACITOR
SRAM/SENSOR CAPACITOR IS REFPESHED BY ON OF CRT AND SFB
SIGNAL LINE POTENTIAL IS SAMPLED TO H-dr
SIGNAL LINE POTENTIAL IS STORED IN EACH SHIFT REGISTER
SHIFT REGISTER STRING IS SINCHRONIZED BY CLOCK AND DATA IS TRANSMITTED BY EACH ONE BIT

FIG. 32

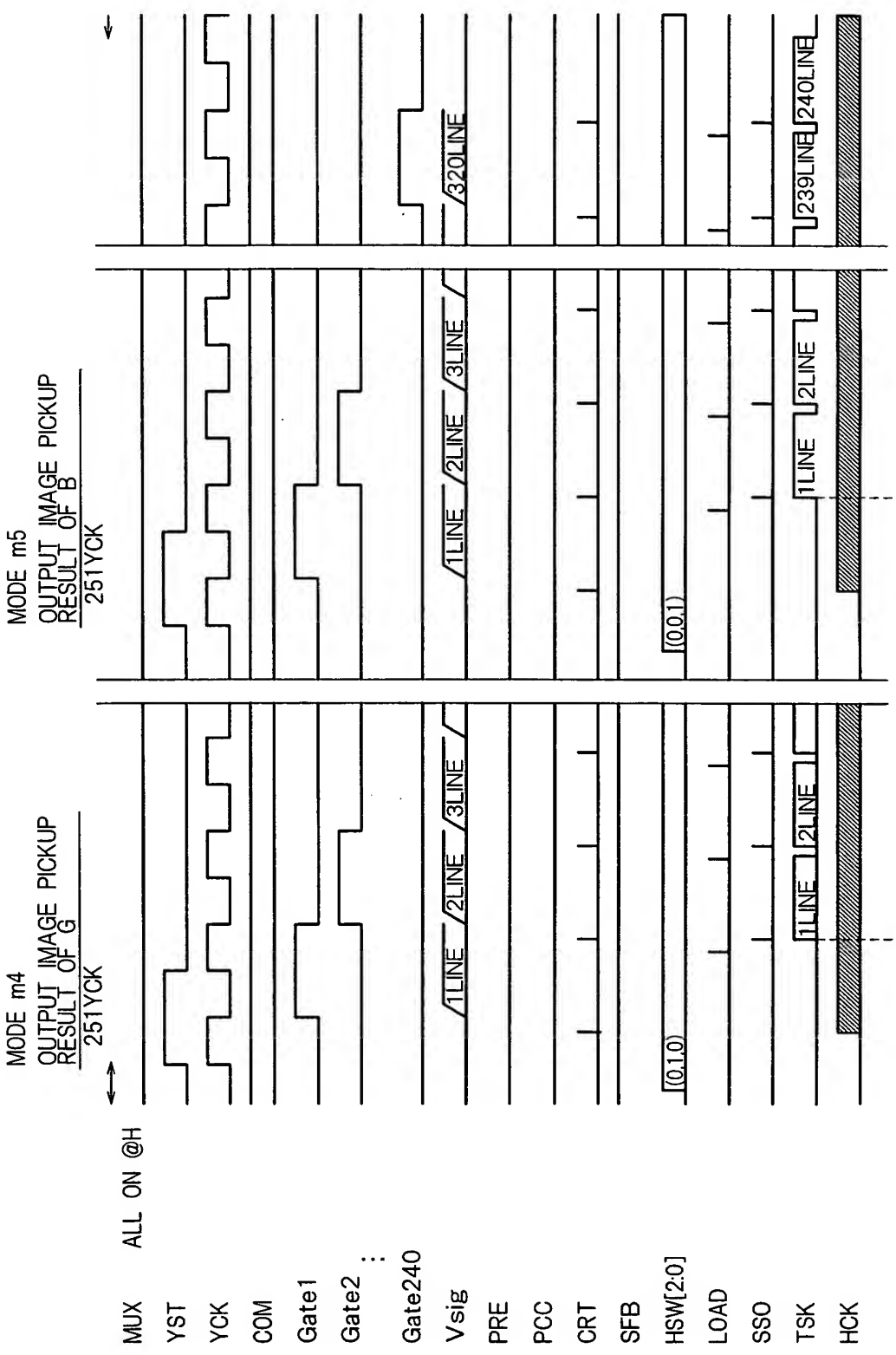

MODE m4
OUTPUT IMAGE PICKUP
RESULT OF G
251YCK
MODE m5
OUTPUT IMAGE PICKUP
RESULT OF B
251YCK
MUX
YST
YCK
COM
Gate1
Gate2
Gate240
Vsig
PRE
PCC
CRT
SFB
HSW[2:0]
LOAD
SSO
TSK
HCK
ALL ON @H
1LINE
2LINE
3LINE
320LINE
239LINE
240LINE
(0,1,0)
(0,0,1)
t7
t8

FIG. 33

1 BLOCK = 40×30
(HORIZONTAL 8, VERTICAL 8)

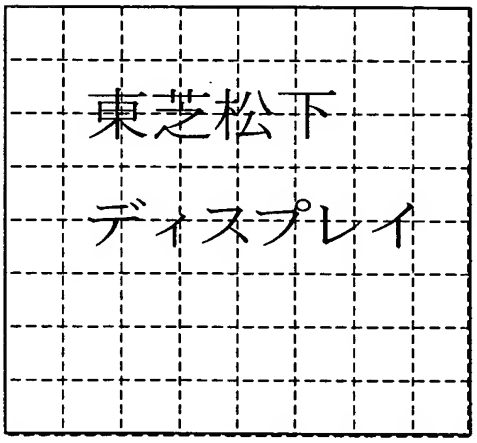


FIG. 34

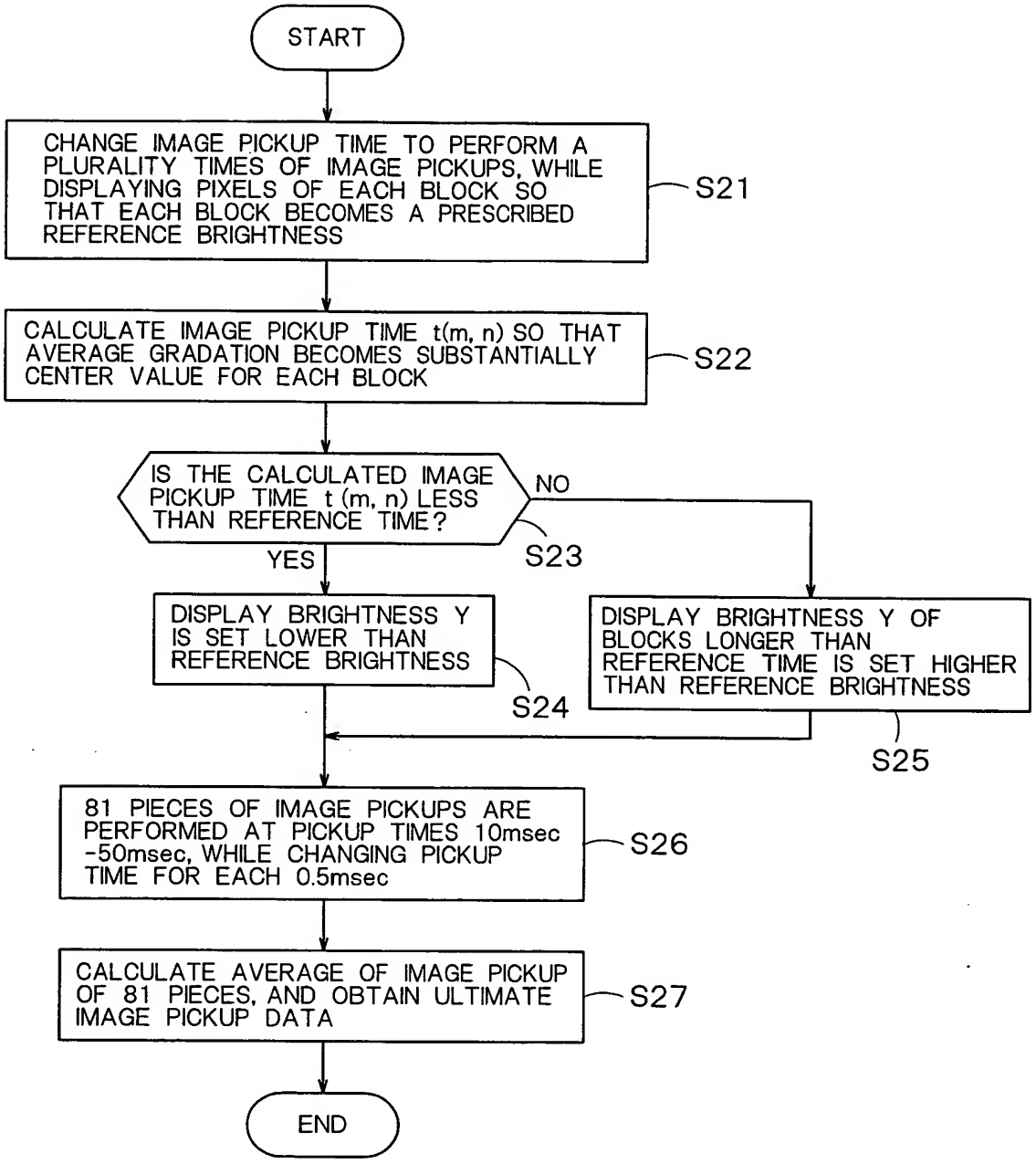

START
CHANGE IMAGE PICKUP TIME TO PERFORM A PLURALITY TIMES OF IMAGE PICKUPS, WHILE DISPLAYING PIXELS OF EACH BLOCK SO THAT EACH BLOCK BECOMES A PRESCRIBED REFERENCE BRIGHTNESS
S21
CALCULATE IMAGE PICKUP TIME t(m, n) SO THAT AVERAGE GRADATION BECOMES SUBSTANTIALLY CENTER VALUE FOR EACH BLOCK
S22
IS THE CALCULATED IMAGE PICKUP TIME t (m, n) LESS THAN REFERENCE TIME?
NO
YES
S23
DISPLAY BRIGHTNESS Y IS SET LOWER THAN REFERENCE BRIGHTNESS
S24
DISPLAY BRIGHTNESS Y OF BLOCKS LONGER THAN REFERENCE TIME IS SET HIGHER THAN REFERENCE BRIGHTNESS
S25
81 PIECES OF IMAGE PICKUPS ARE PERFORMED AT PICKUP TIMES 10msec -50msec, WHILE CHANGING PICKUP TIME FOR EACH 0.5msec
S26
CALCULATE AVERAGE OF IMAGE PICKUP OF 81 PIECES, AND OBTAIN ULTIMATE IMAGE PICKUP DATA
S27
END

FIG. 35

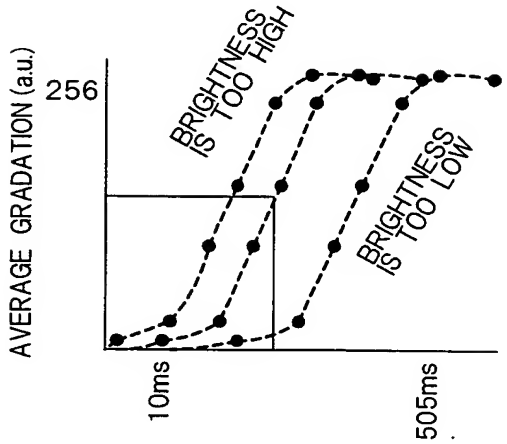


FIG. 36

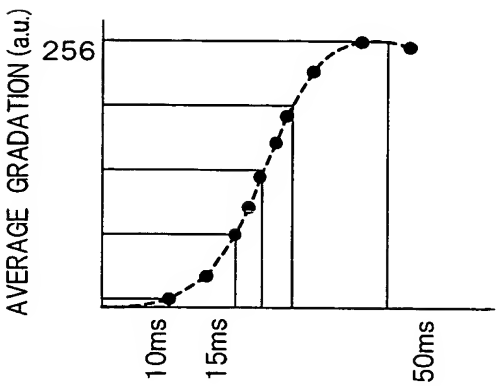


FIG. 37

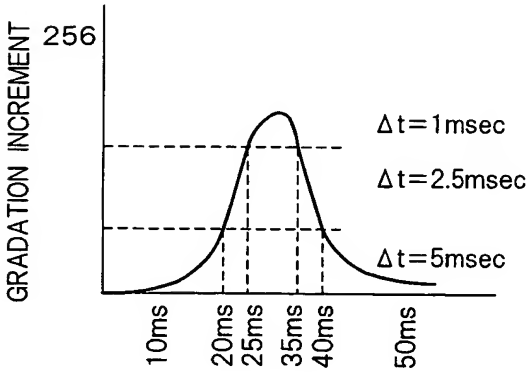


FIG. 38

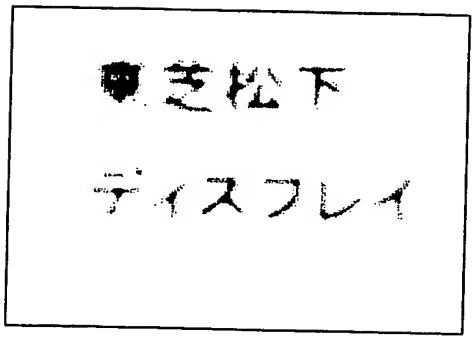


FIG. 39

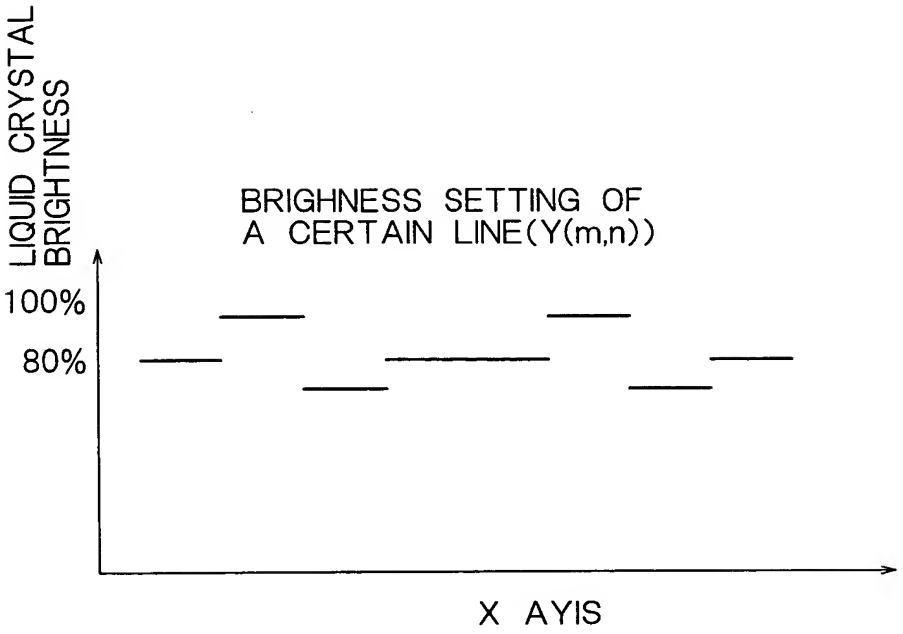

LIQUID CRYSTAL BRIGHTNESS
BRIGHNESS SETTING OF A CERTAIN LINE(Y(m,n))
100%
80%
X AYIS

FIG. 40

FIG. 41

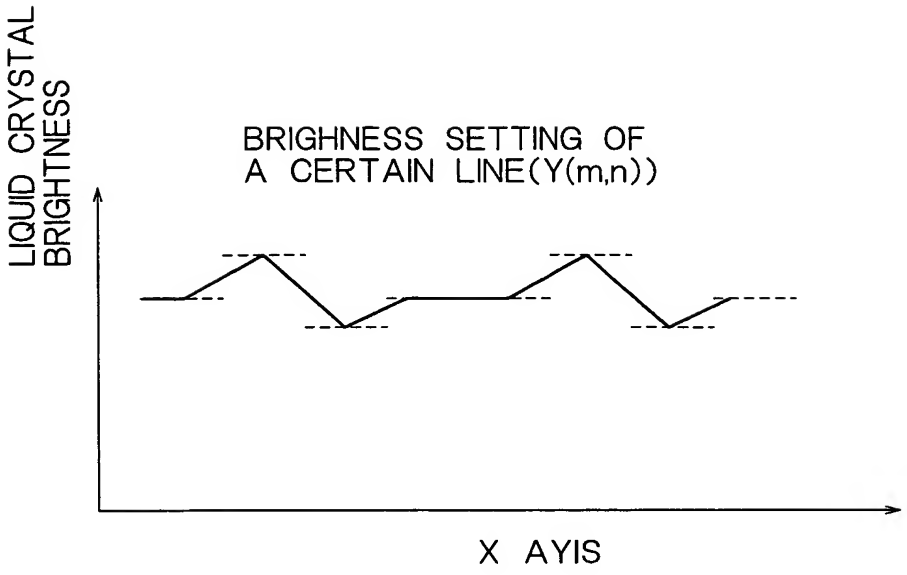

LIQUID CRYSTAL BRIGHTNESS
BRIGHNESS SETTING OF A CERTAIN LINE(Y(m,n))
X AYIS

FIG. 42

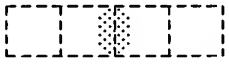


FIG. 43

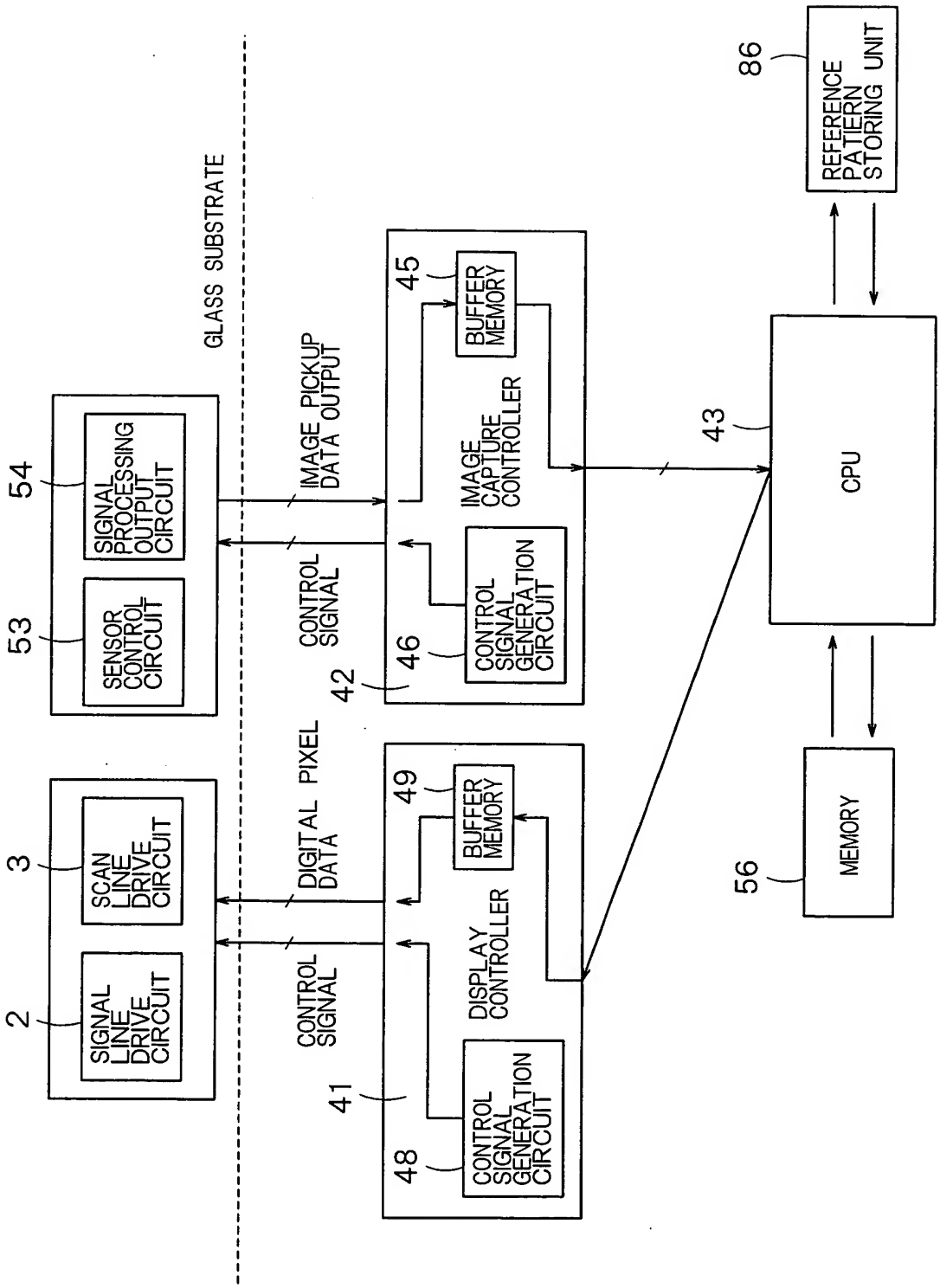

GLASS SUBSTRATE
2
SIGNAL LINE DRIVE CIRCUIT
3
SCAN LINE DRIVE CIRCUIT
53
SENSOR CONTROL CIRCUIT
54
SIGNAL PROCESSING OUTPUT CIRCUIT
DIGITAL PIXEL DATA
CONTROL SIGNAL
IMAGE PICKUP DATA OUTPUT
CONTROL SIGNAL
41
DISPLAY CONTROLLER
48
CONTROL SIGNAL GENERATION CIRCUIT
49
BUFFER MEMORY
42
IMAGE CAPTURE CONTROLLER
46
CONTROL SIGNAL GENERATION CIRCUIT
45
BUFFER MEMORY
43
CPU
56
MEMORY
86
REFERENCE PATTERN STORING UNIT

FIG. 44

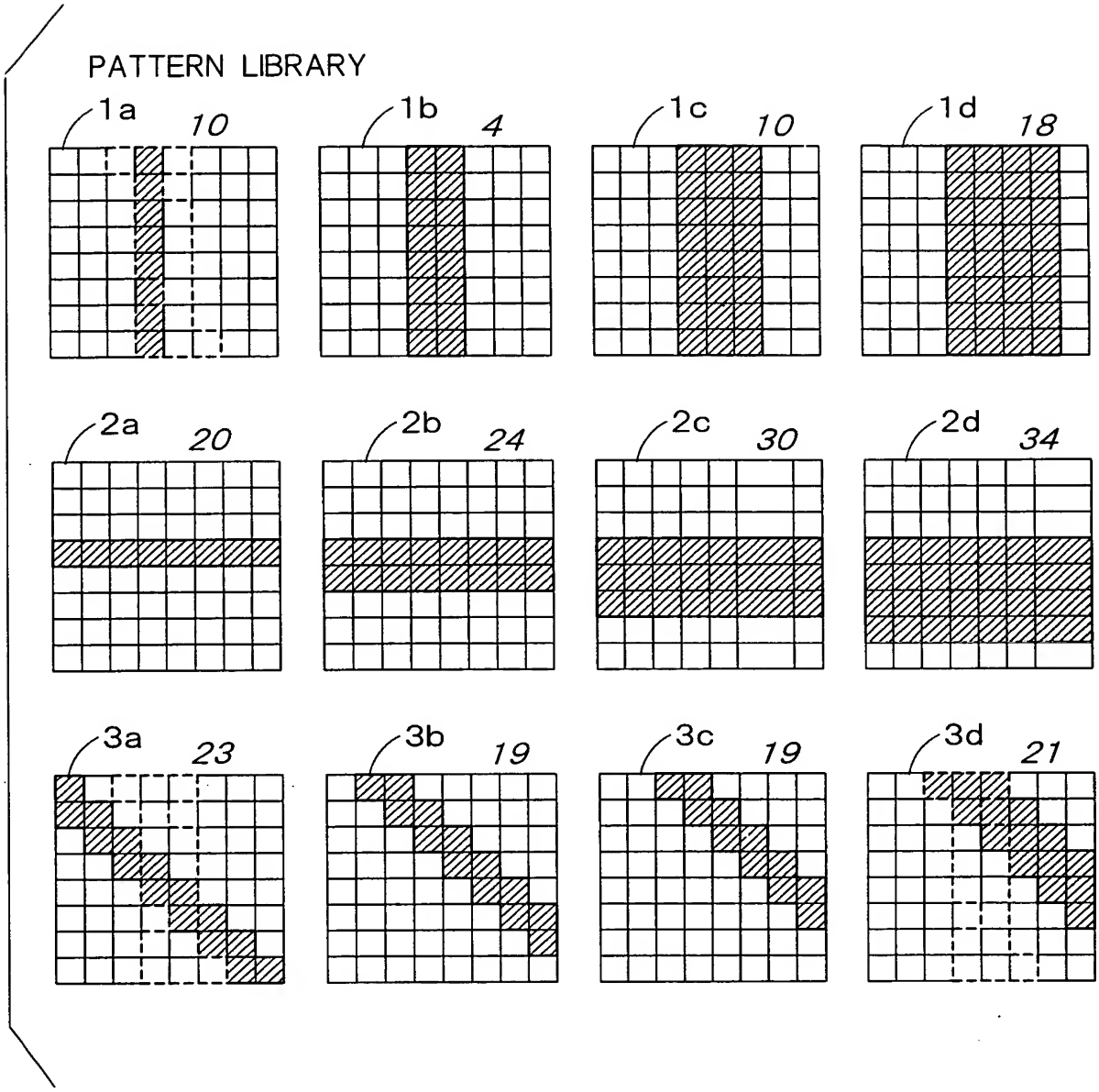

PATTERN LIBRARY
1a
10
1b
4
1c
10
1d
18
2a
20
2b
24
2c
30
2d
34
3a
23
3b
19
3c
19
3d
21

FIG. 45

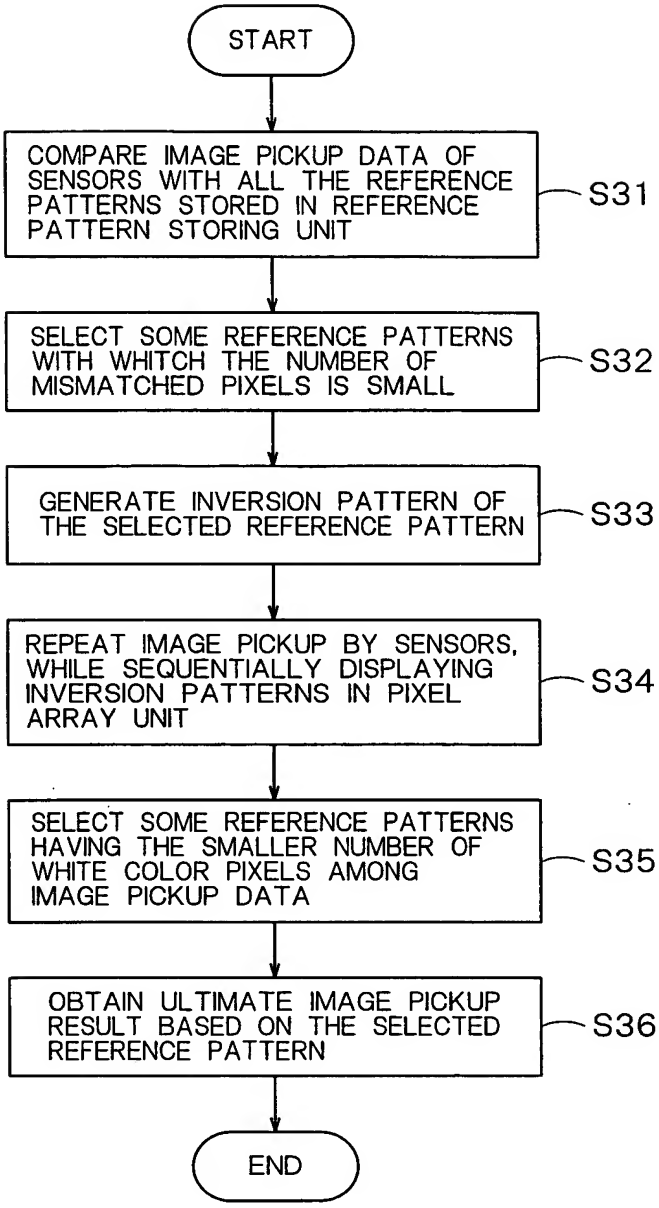

START
COMPARE IMAGE PICKUP DATA OF SENSORS WITH ALL THE REFERENCE PATTERNS STORED IN REFERENCE PATTERN STORING UNIT
S31
SELECT SOME REFERENCE PATTERNS WITH WHITCH THE NUMBER OF MISMATCHED PIXELS IS SMALL
S32
GENERATE INVERSION PATTERN OF THE SELECTED REFERENCE PATTERN
S33
REPEAT IMAGE PICKUP BY SENSORS, WHILE SEQUENTIALLY DISPLAYING INVERSION PATTERNS IN PIXEL ARRAY UNIT
S34
SELECT SOME REFERENCE PATTERNS HAVING THE SMALLER NUMBER OF WHITE COLOR PIXELS AMONG IMAGE PICKUP DATA
S35
OBTAIN ULTIMATE IMAGE PICKUP RESULT BASED ON THE SELECTED REFERENCE PATTERN
S36
END

FIG. 46

IMAGE PICKUP OBJECT

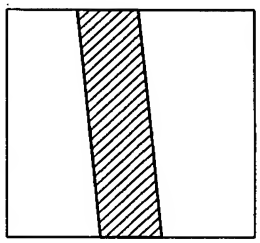


FIG. 47

IMAGE PICKUP RESULT

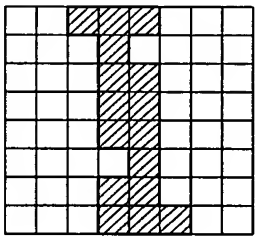


FIG. 48

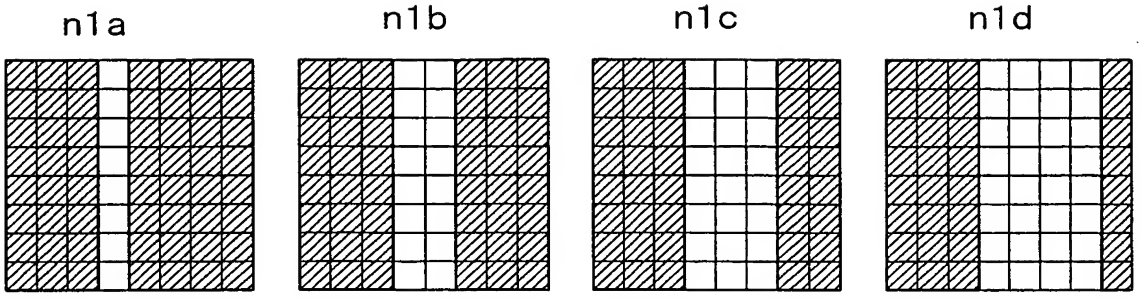


FIG. 49

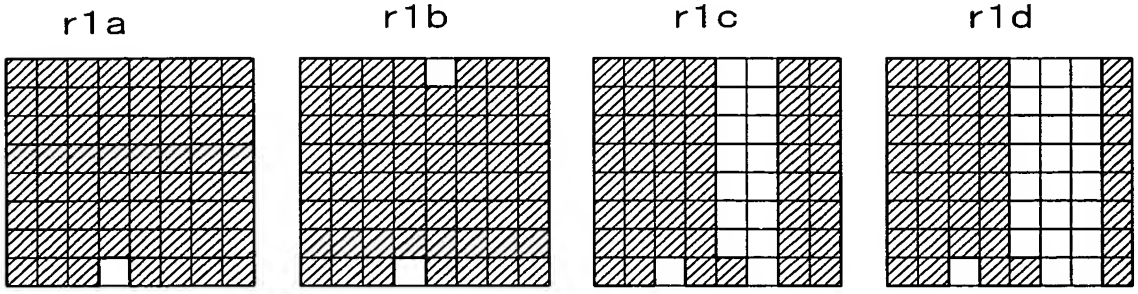


FIG. 50

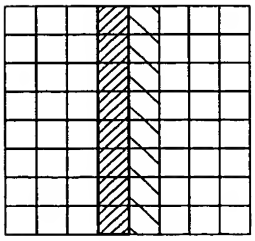


FIG. 51

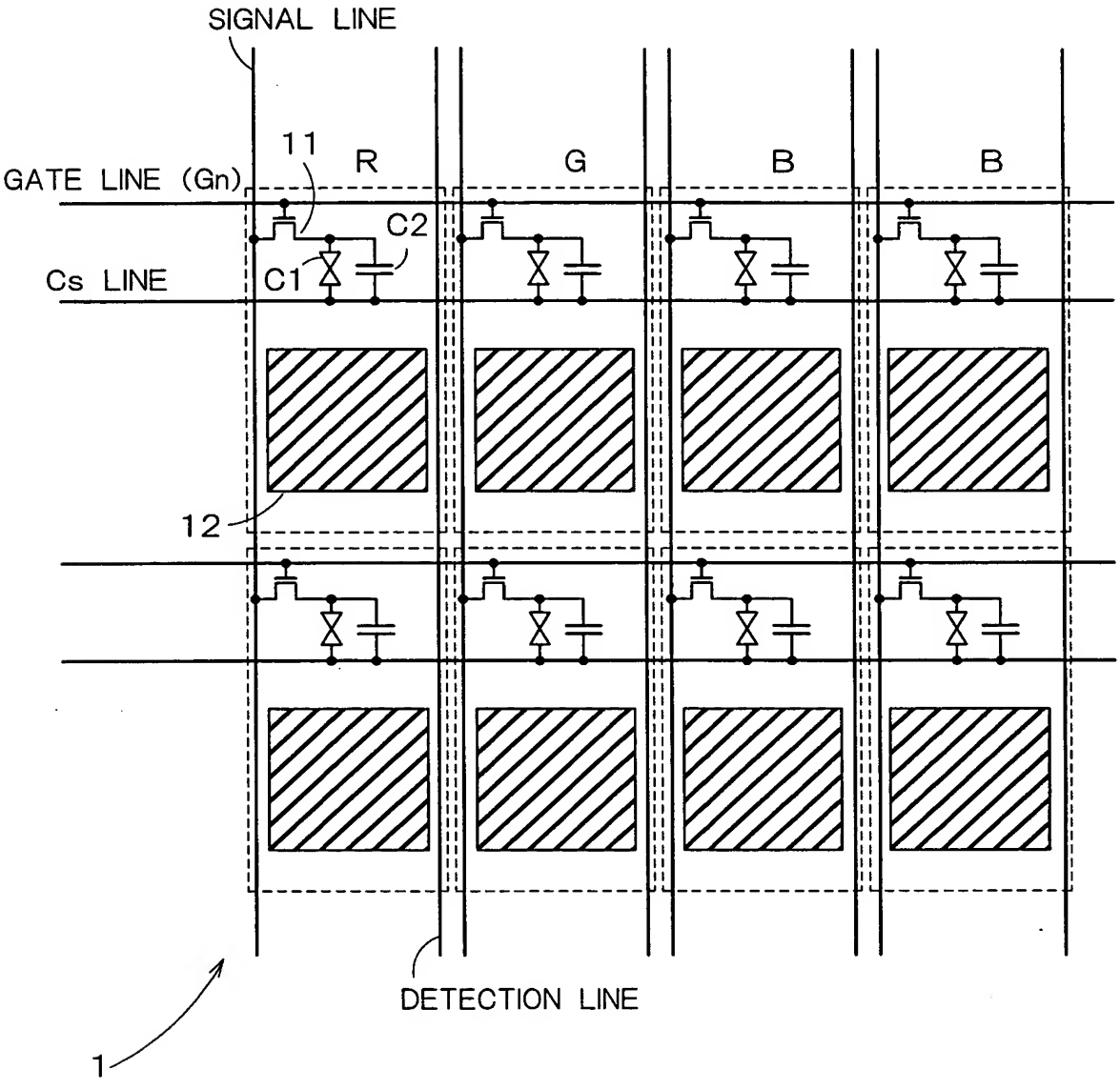

SIGNAL LINE
11
R
G
B
B
GATE LINE (Gn)
C2
C1
Cs LINE
12
DETECTION LINE
1

FIG. 52

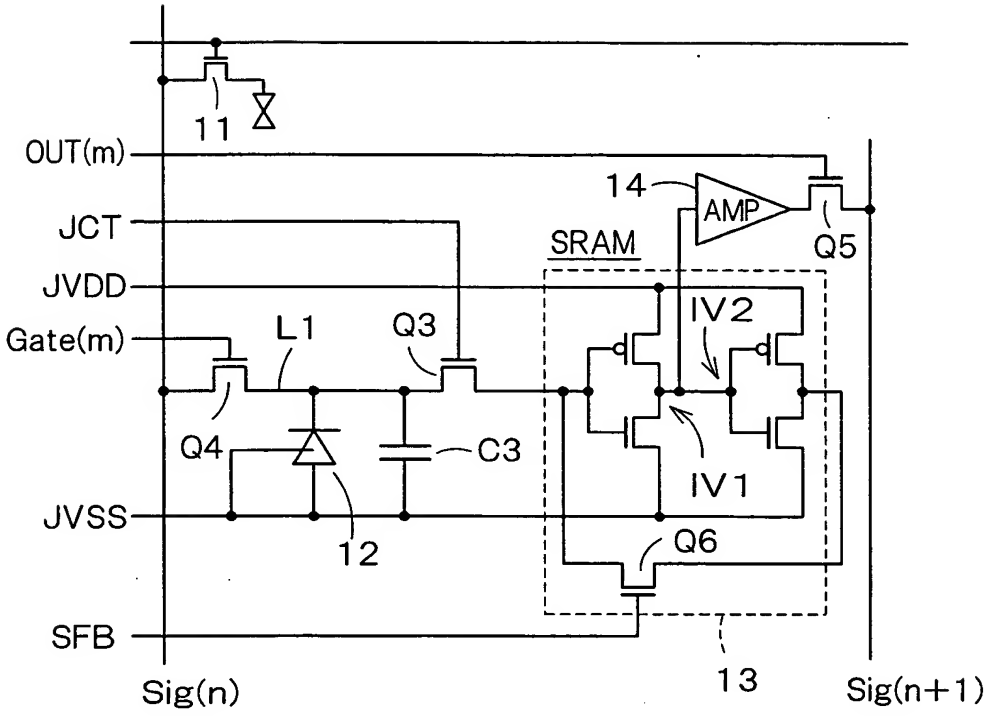

11
OUT(m)
JCT
JVDD
Gate(m)
JVSS
SFB
Sig(n)
L1
Q3
Q4
C3
12
14
AMP
SRAM
Q5
IV2
IV1
Q6
13
Sig(n+1)

FIG. 53

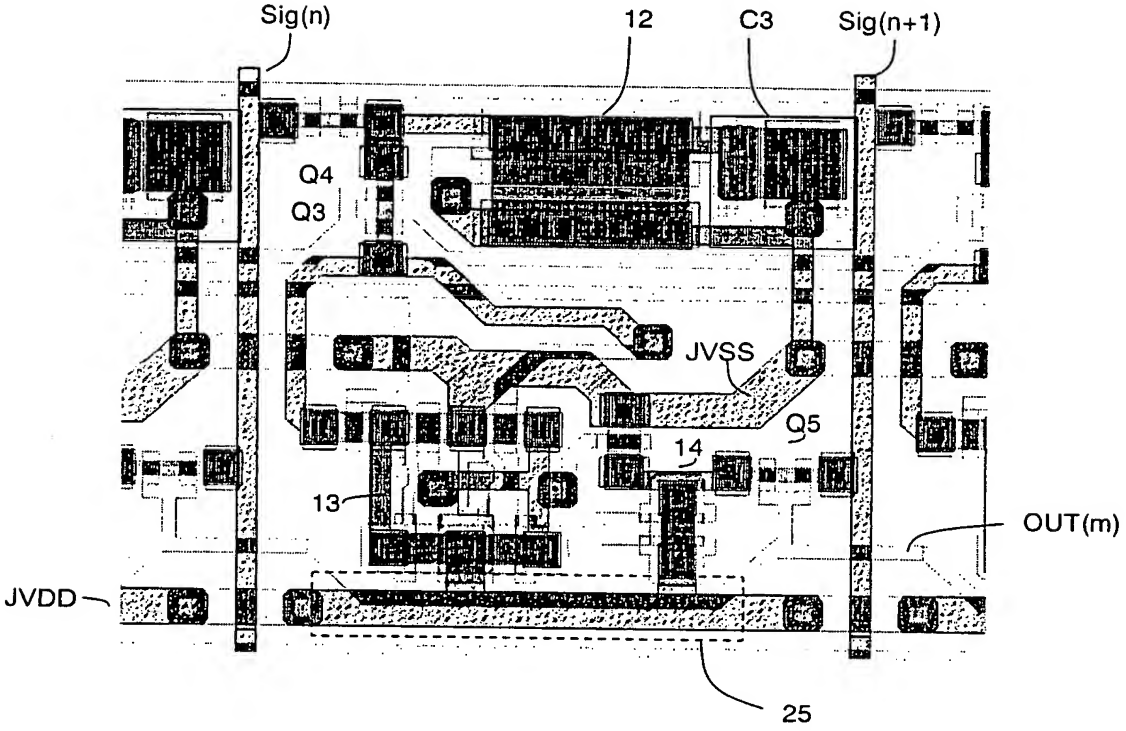
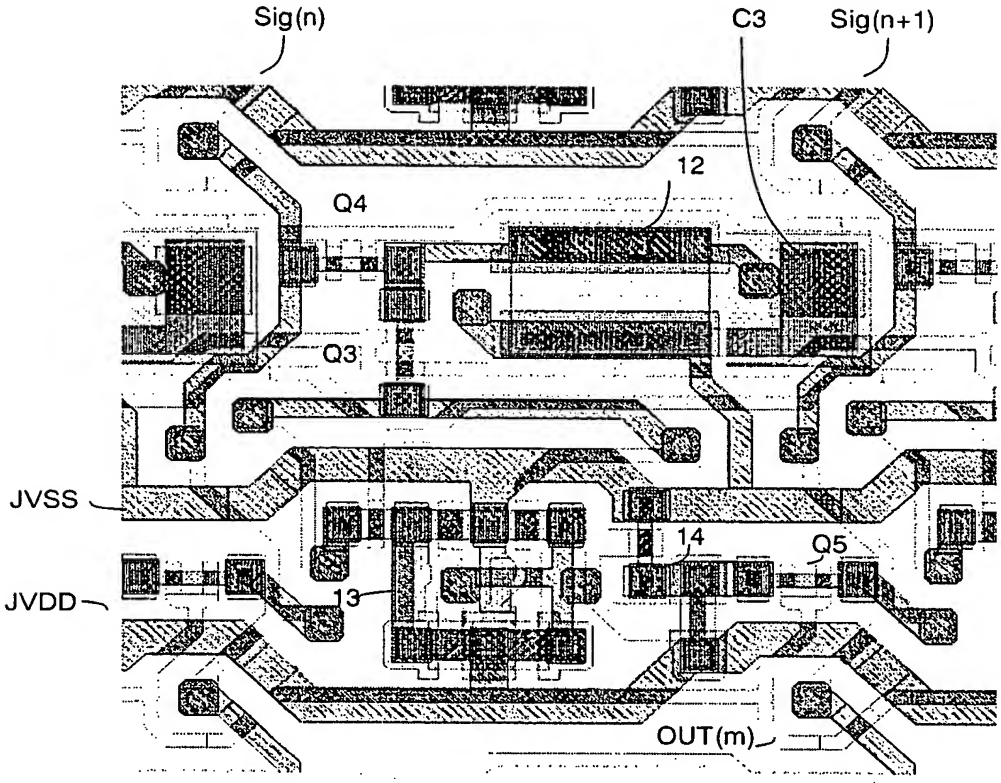


FIG. 54



JVDD, JVSS···PATTERNED BY ONLY FIRST METAL

Sig(n)···PATTERNED BY CONNECTING FIRST AND SECOND METALS TO EACH OTHER

FIG. 55

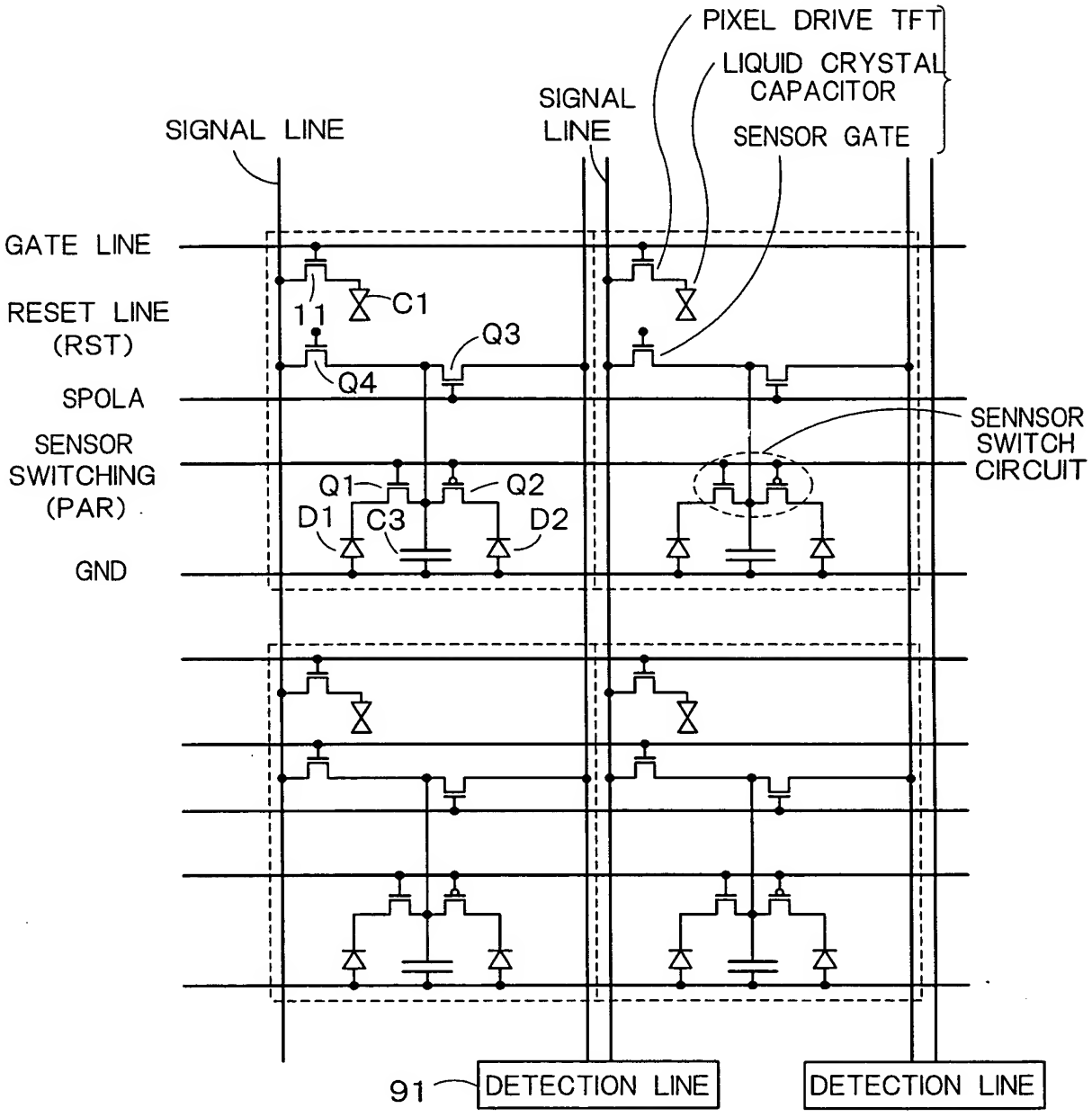

PIXEL DRIVE TFT
LIQUID CRYSTAL CAPACITOR
SENSOR GATE
SIGNAL LINE
SIGNAL LINE
GATE LINE
RESET LINE (RST)
SPOLA
SENSOR SWITCHING (PAR)
GND
11
C1
Q3
Q4
Q1
Q2
D1
C3
D2
SENNSOR SWITCH CIRCUIT
91
DETECTION LINE
DETECTION LINE

FIG. 56

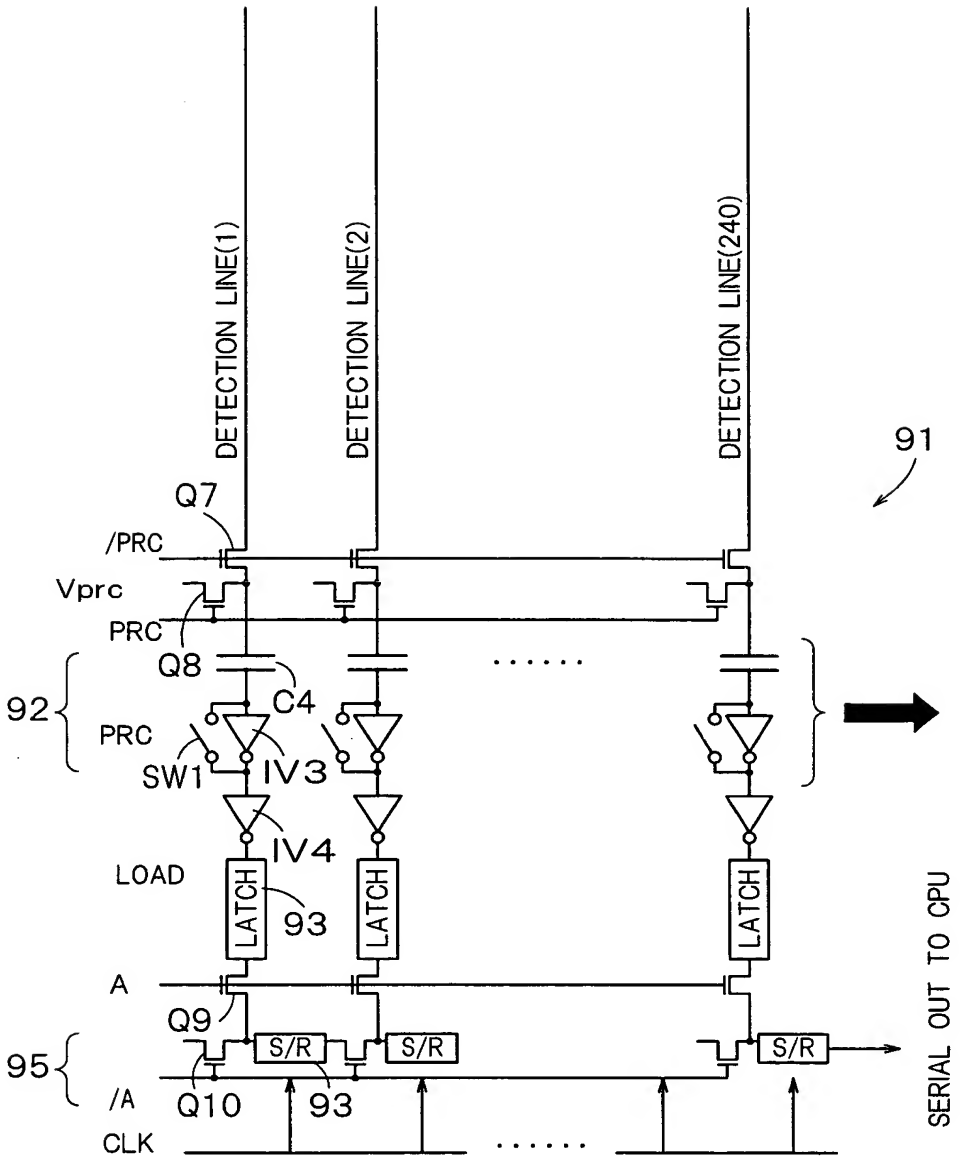

DETECTION LINE(1)
DETECTION LINE(2)
DETECTION LINE(240)
91
Q7
/PRC
Vprc
PRC
Q8
C4
92
PRC
SW1
IV3
IV4
LOAD
LATCH
93
A
Q9
S/R
95
/A
Q10
CLK
SERIAL OUT TO CPU

FIG. 57

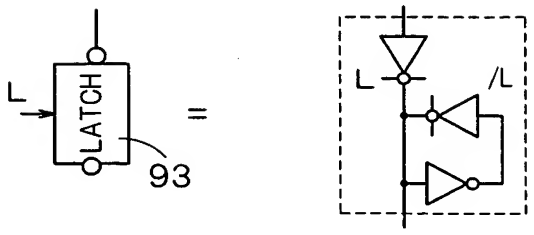


FIG. 58A

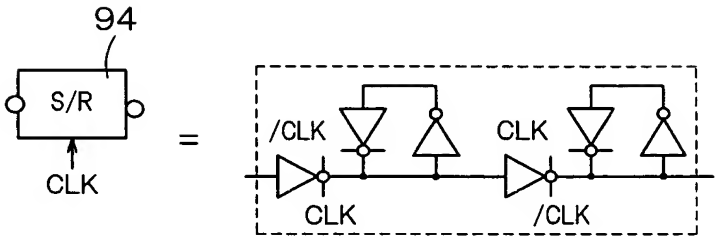


FIG. 58B

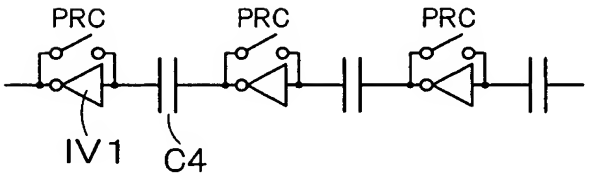


FIG. 59

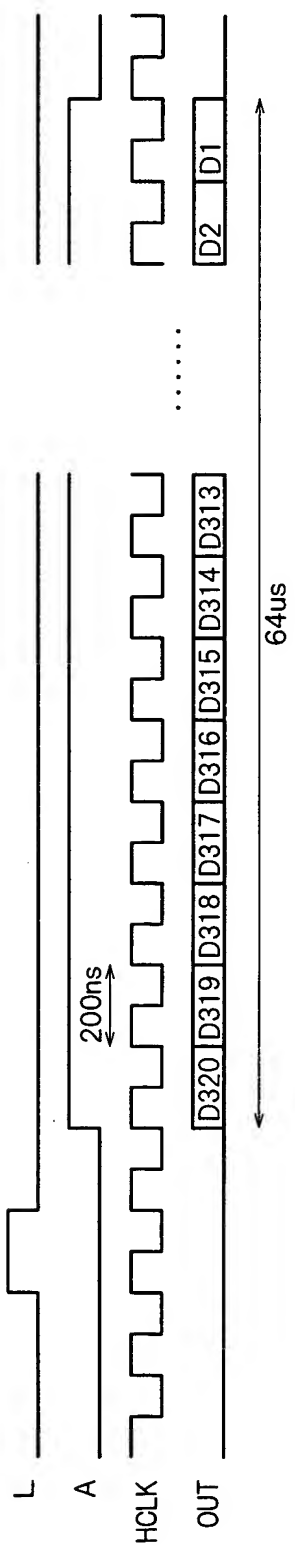

L
A
HCLK
OUT
200ns
D320
D319
D318
D317
D316
D315
D314
D313
D2
D1
64us

FIG. 60

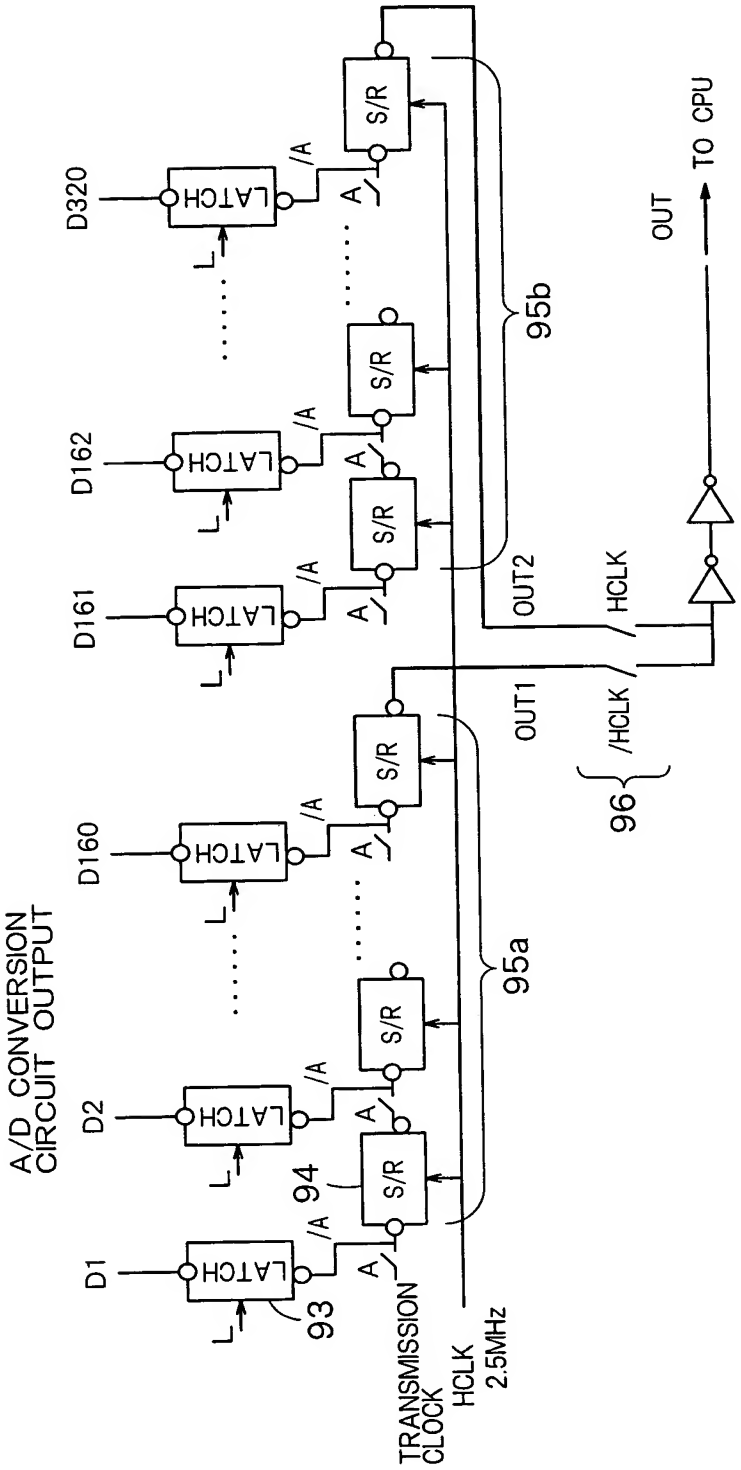

A/D CONVERSION CIRCUIT OUTPUT
D1
D2
D160
D161
D162
D320
LATCH
L
/A
A
S/R
93
94
95a
95b
96
OUT1
OUT2
HCLK
/HCLK
TRANSMISSION CLOCK
HCLK 2.5MHz
OUT
TO CPU

FIG. 61

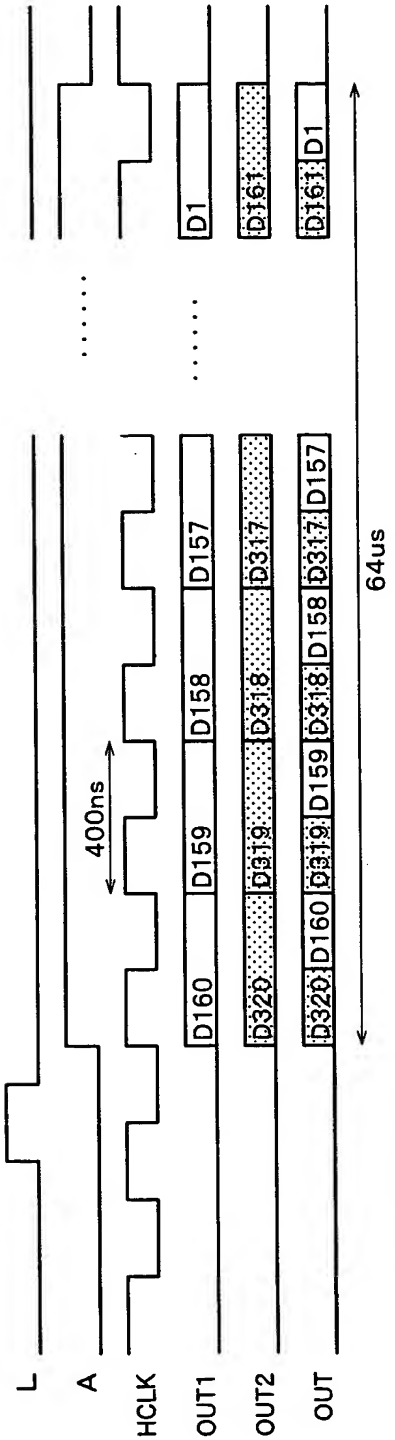

L
A
HCLK
OUT1
OUT2
OUT
400ns
64us
D160
D159
D158
D157
D320
D319
D318
D317
D161
D1

FIG. 62

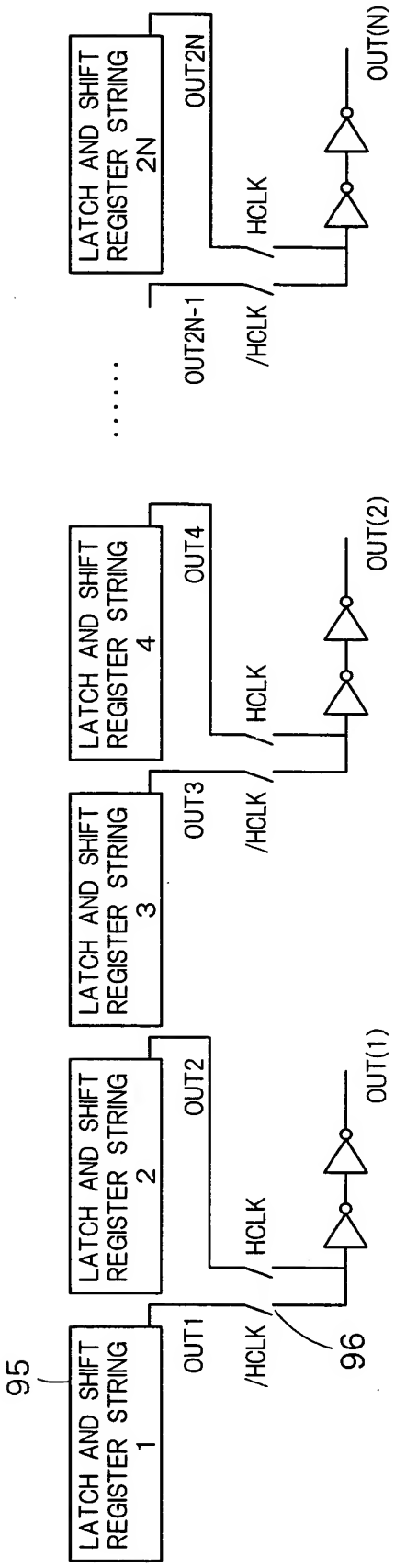

95
LATCH AND SHIFT REGISTER STRING 1
LATCH AND SHIFT REGISTER STRING 2
LATCH AND SHIFT REGISTER STRING 3
LATCH AND SHIFT REGISTER STRING 4
LATCH AND SHIFT REGISTER STRING 2N
OUT1
OUT2
OUT3
OUT4
OUT2N-1
OUT2N
/HCLK
HCLK
96
OUT(1)
OUT(2)
OUT(N)

FIG. 63

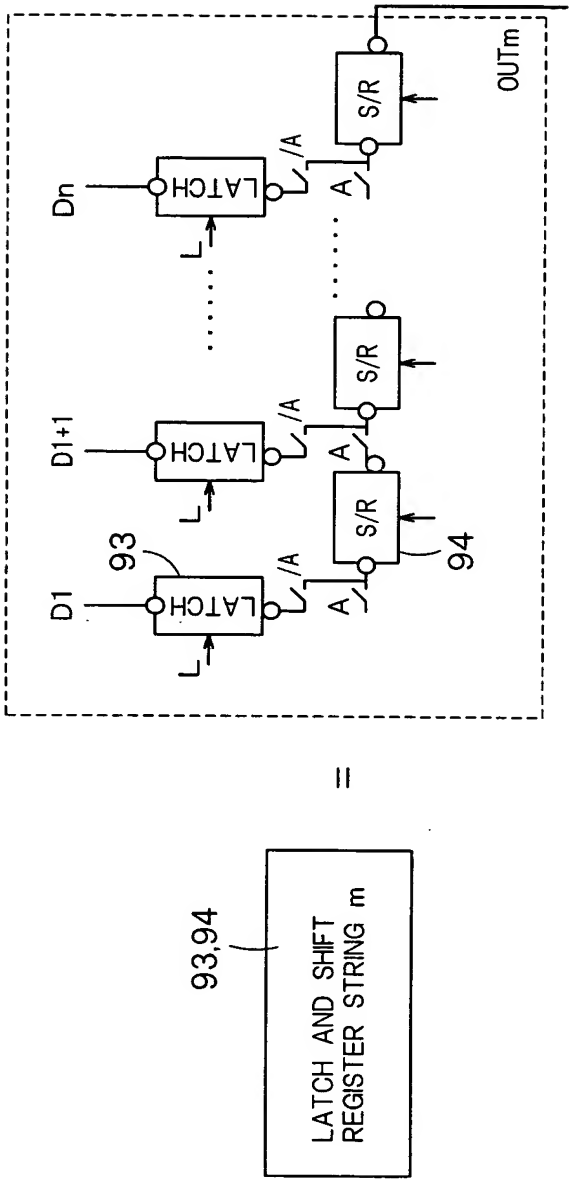

OUTm
S/R
/A
A
LATCH
Dn
D1+1
D1
93
94
L
.....
=
93,94
LATCH AND SHIFT REGISTER STRING m

FIG. 64

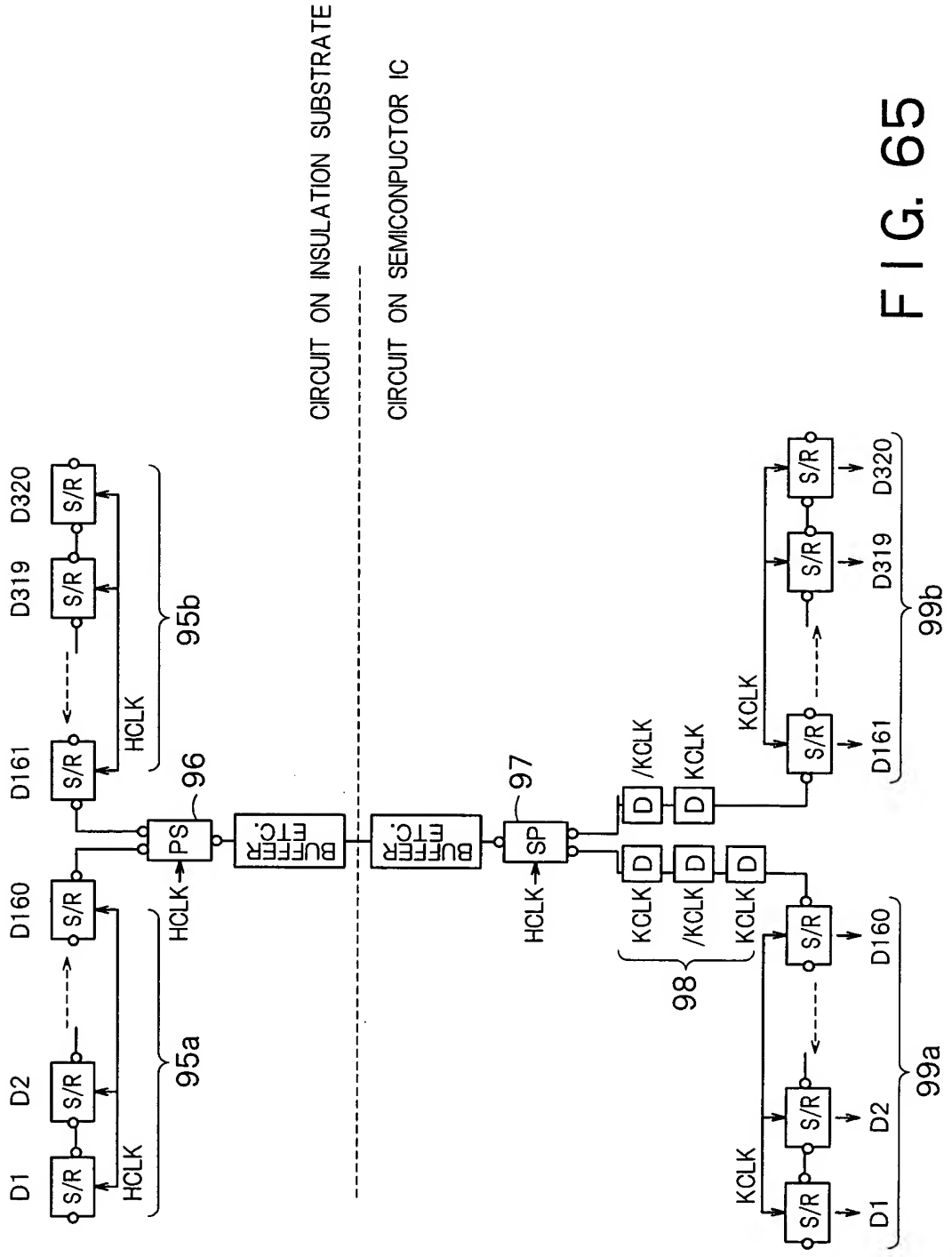

CIRCUIT ON INSULATION SUBSTRATE
CIRCUIT ON SEMICONPUCTOR IC
D1
D2
D160
D161
D319
D320
S/R
HCLK
95a
95b
PS
96
BUFFER ETC.
97
SP
98
KCLK
/KCLK
D
99a
99b

FIG. 65

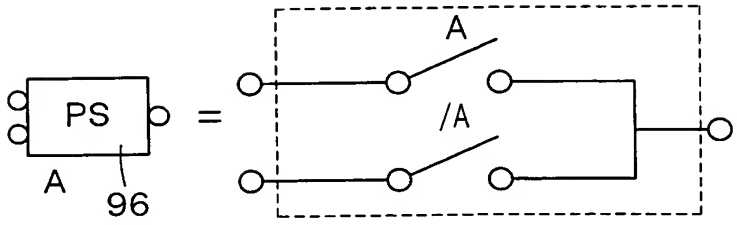


FIG. 66A

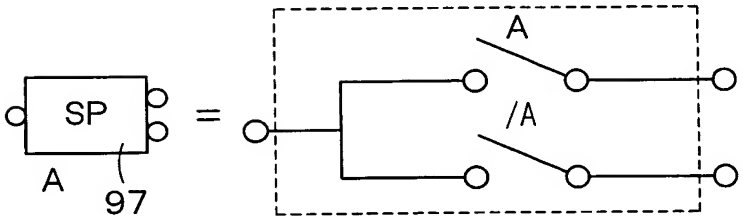


FIG. 66B

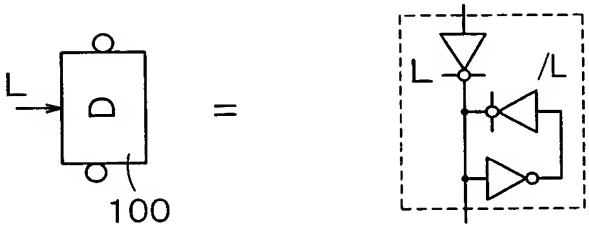


FIG. 67

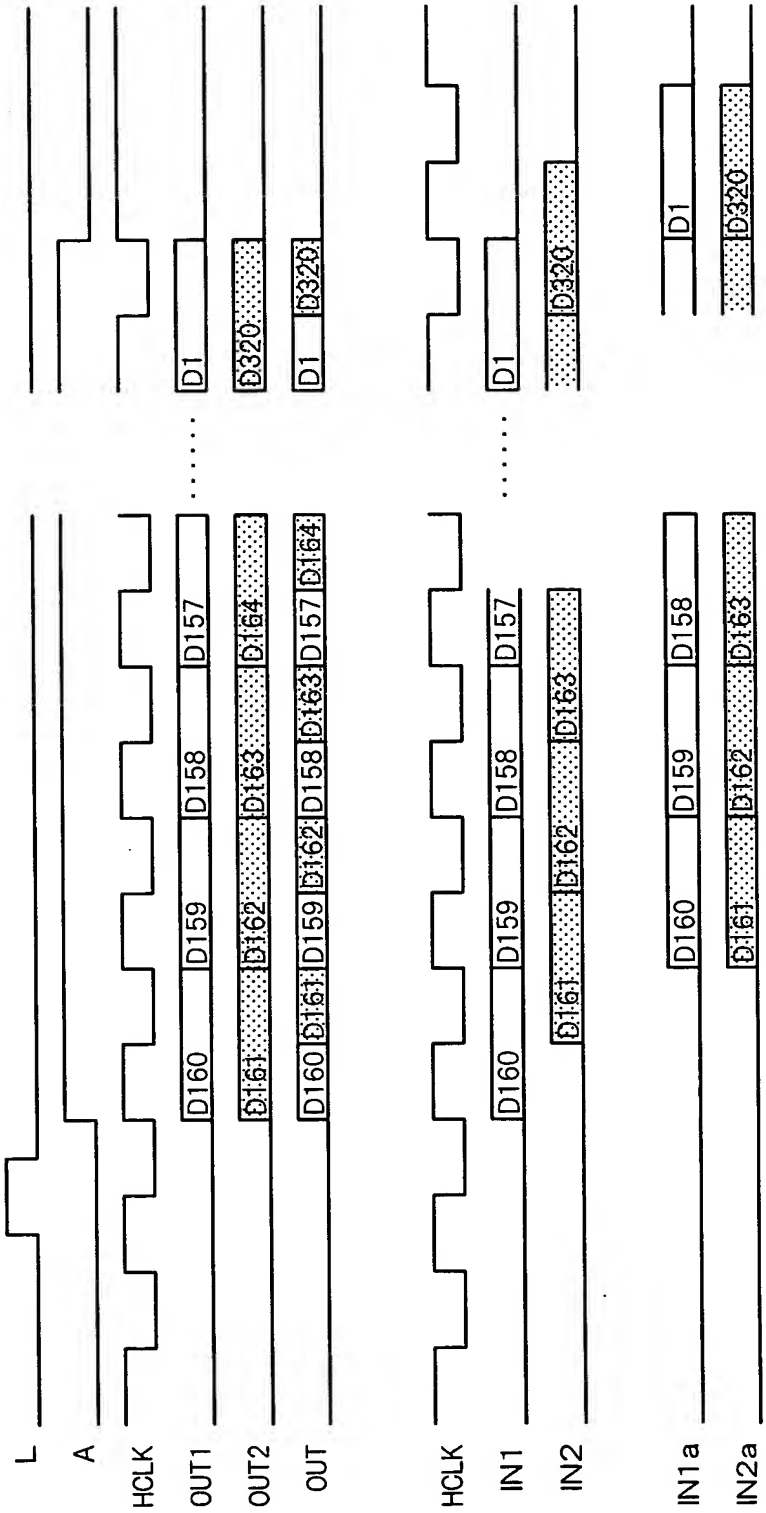

L
A
HCLK
OUT1
OUT2
OUT
HCLK
IN1
IN2
IN1a
IN2a
D1
D320
D160
D159
D158
D157
D162
D163
D164
D161

FIG. 68

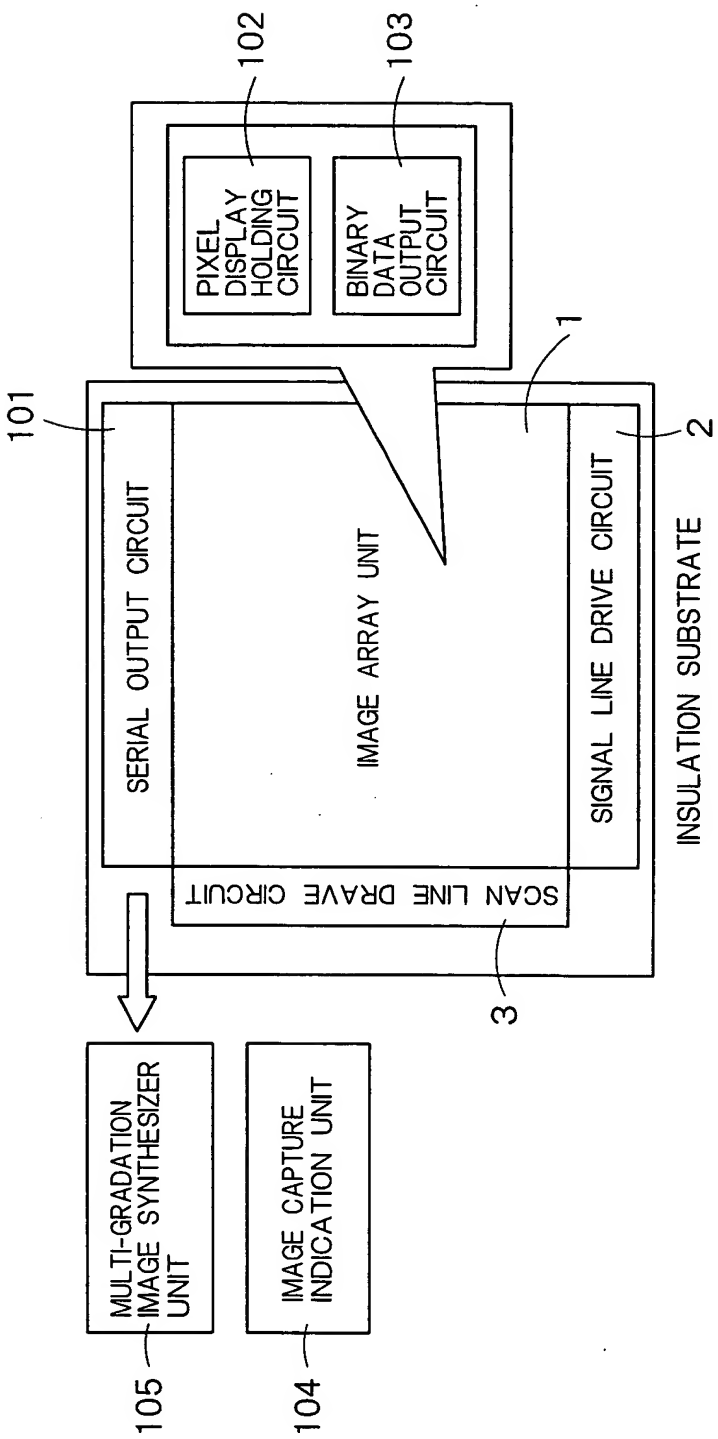

102
103
PIXEL DISPLAY HOLDING CIRCUIT
BINARY DATA OUTPUT CIRCUIT
1
101
2
SERIAL OUTPUT CIRCUIT
IMAGE ARRAY UNIT
SIGNAL LINE DRIVE CIRCUIT
INSULATION SUBSTRATE
SCAN LINE DRAVE CIRCUIT
3
MULTI-GRADATION IMAGE SYNTHESIZER UNIT
IMAGE CAPTURE INDICATION UNIT
105
104

FIG. 69

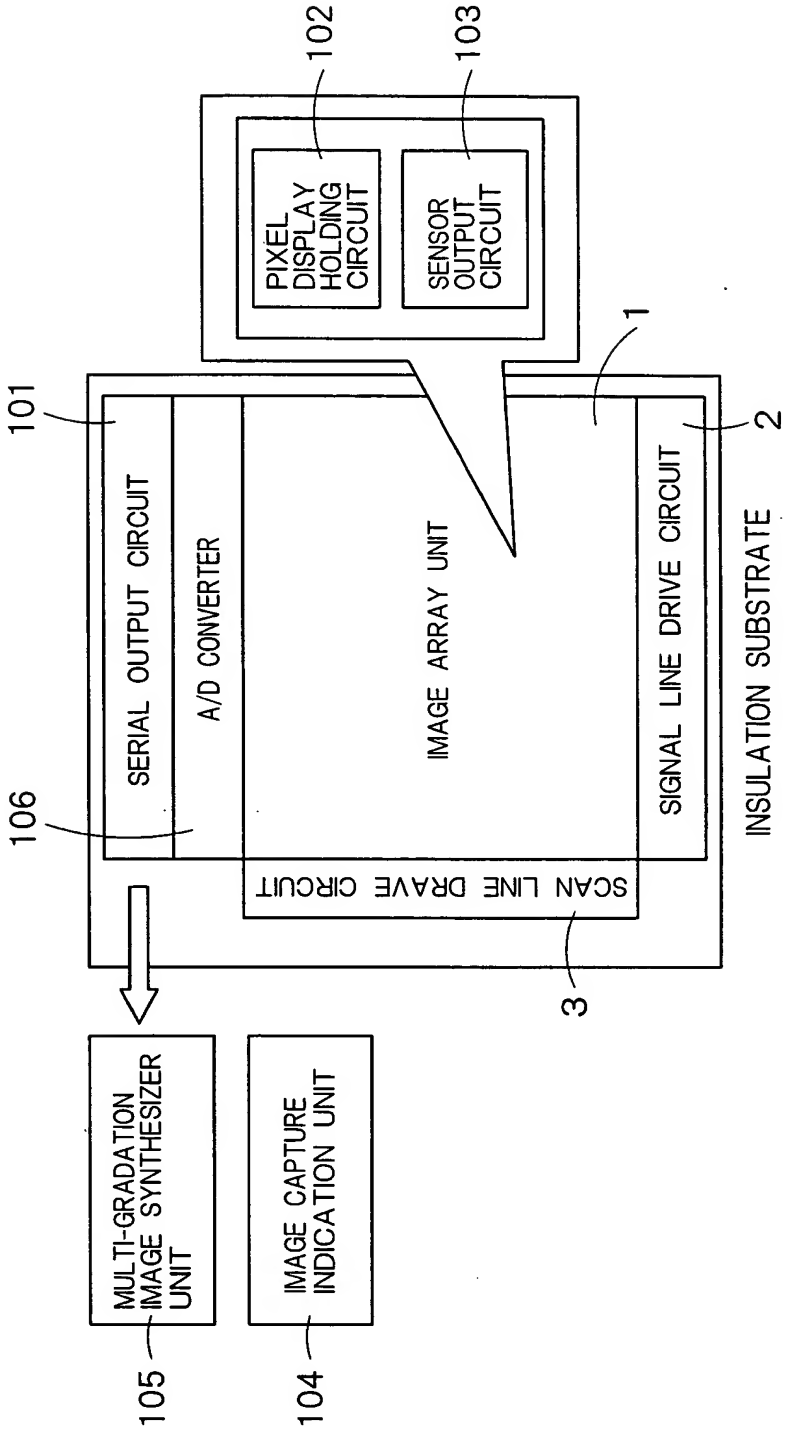

102
103
PIXEL DISPLAY HOLDING CIRCUIT
SENSOR OUTPUT CIRCUIT
1
101
2
SERIAL OUTPUT CIRCUIT
A/D CONVERTER
IMAGE ARRAY UNIT
SIGNAL LINE DRIVE CIRCUIT
INSULATION SUBSTRATE
106
SCAN LINE DRAVE CIRCUIT
3
MULTI-GRADATION IMAGE SYNTHESIZER UNIT
IMAGE CAPTURE INDICATION UNIT
105
104

FIG. 70

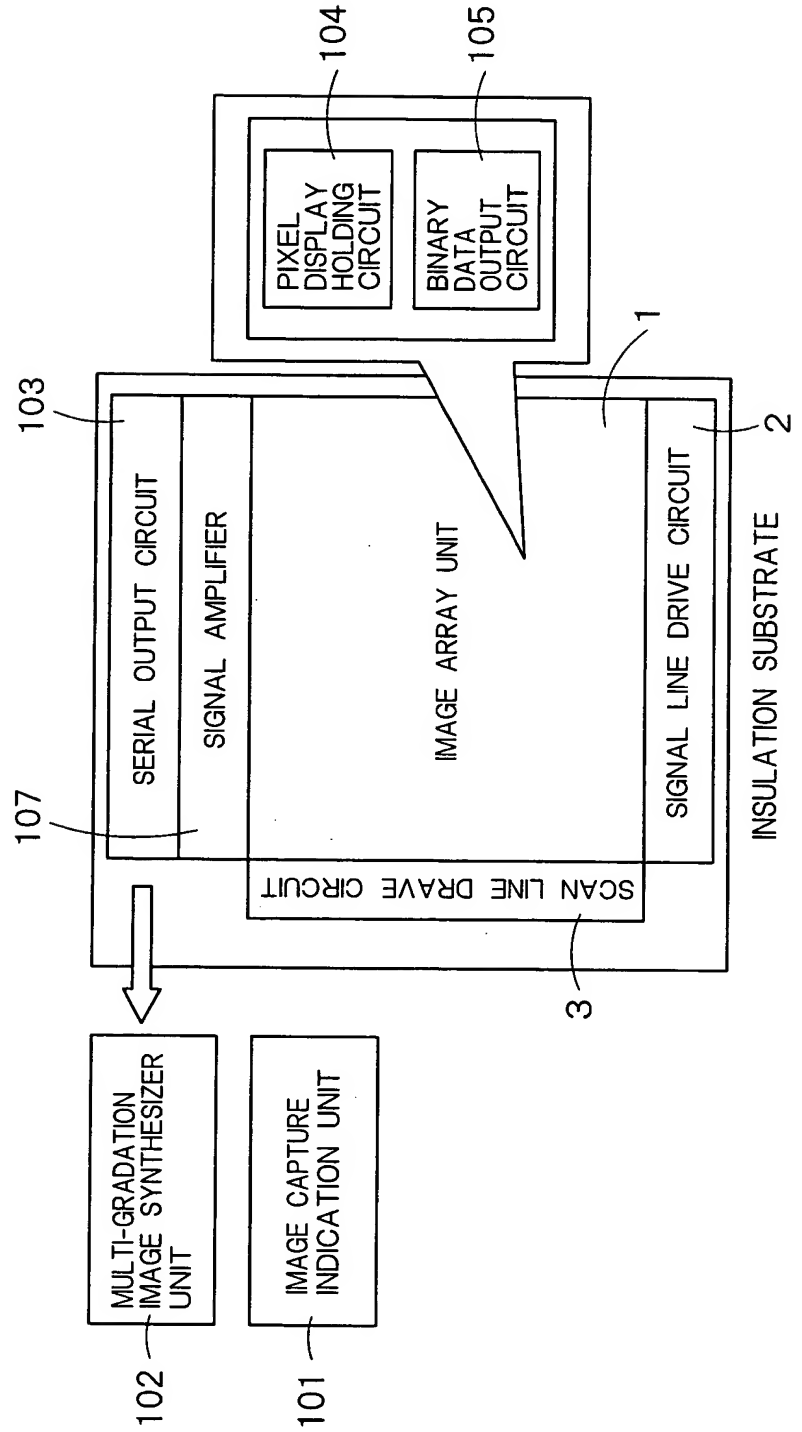

104
105
PIXEL DISPLAY HOLDING CIRCUIT
BINARY DATA OUTPUT CIRCUIT
1
103
SERIAL OUTPUT CIRCUIT
SIGNAL AMPLIFIER
IMAGE ARRAY UNIT
SIGNAL LINE DRIVE CIRCUIT
2
INSULATION SUBSTRATE
107
SCAN LINE DRAVE CIRCUIT
3
MULTI-GRADATION IMAGE SYNTHESIZER UNIT
IMAGE CAPTURE INDICATION UNIT
102
101

FIG. 71